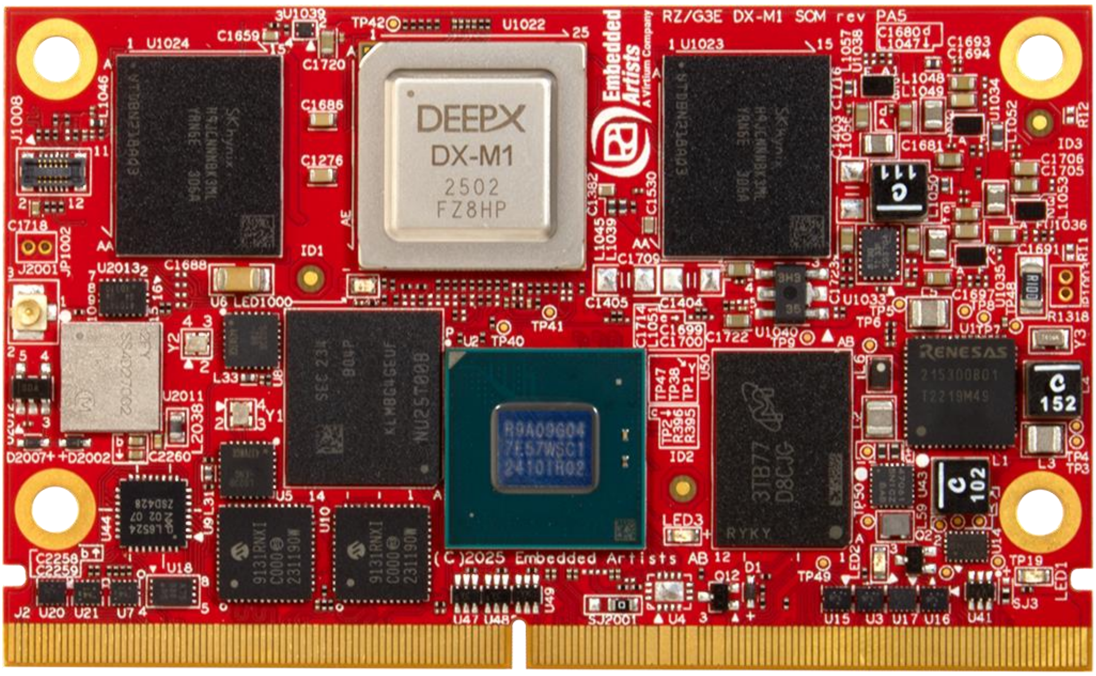
RZ/G3E DX-M1 SOM and RZ/G3E SOM Datasheet



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1 Document Information

This document applies to several products, differentiated by mounting option. This table below lists the product differences. All products are not stocked. Consult Embedded Artists for availability, lead time, and other mounting options.

Type Number	*Product Name*	*Cortex-A55 Frequency*	*SDRAM/ eMMC*	*NPU RAM*	*Wi-Fi/ BT*	*Operating Temperature*
EAC00529	RZ/G3E DX-M1 SOM	1.8 GHz	4/64 GByte	4 GByte	No	0 -70°C
EAC00530	RZ/G3E DX-M1 SOM	1.8 GHz	4/64 GByte	4 GByte	No	-40 -85°C
EAC005xx	RZ/G3E DX-M1 SOM	1.8 GHz	2/16 GByte	2 GByte	No	0 -70°C
EAC005xx	RZ/G3E DX-M1 SOM	1.8 GHz	2/16 GByte	2 GByte	No	-40 -85°C
EAC00527	RZ/G3E SOM	1.8 GHz	2/16 GByte	No DX-M1	No	0 -70°C
EAC00528	RZ/G3E SOM	1.8 GHz	2/16 GByte	No DX-M1	No	-40 -85°C
EAC00559	RZ/G3E SOM	1.8 GHz	1/8 GByte	No DX-M1	No	0 -70°C
EAC00560	RZ/G3E SOM	1.8 GHz	1/8 GByte	No DX-M1	No	-40 -85°C

1.1 Revision History

Revision	*Date*	*Description*
PA1	2026-03-16	First version.

2 Introduction

This document is a datasheet that specifies and describes the *RZ/G3E DX-M1 SOM Board* and *RZ/G3E SOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

Note that both versions of the board; *RZ/G3E DX-M1 SOM Board* and *RZ/G3E SOM Board* will be jointly referred to as ***RZ/G3E (DX-M1) SOM Board*** in this document.

2.1 Hardware

The *RZ/G3E (DX-M1) SOM Board* is a System-on-Module (SOM) based on Renesas's ARM quad-core Cortex-A55 / single-core Cortex-M33 RZ/G3E System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A55 / M33 based design. The Cortex-A55 cores run up to 1.8 GHz and the Cortex-M33 core at up to 200 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A55 cores and a Real-Time OS (RTOS) on the Cortex-M33. This architecture is ideal for real time applications where Linux cannot be used for all time critical tasks. The Cortex-M33 can manage (real time) critical tasks and can also be used to lower power consumption.

The *RZ/G3E (DX-M1) SOM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR4 memory sub-system reduces the power consumption.

The *RZ/G3E (DX-M1) SOM Board* has a small form factor and shields the user from a lot of complexity of designing a high-performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *RZ/G3E (DX-M1) SOM Board* targets a wide range of applications, such as:

- Edge Compute applications
- Edge AI applications
- HMI/GUI solutions
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *RZ/G3E (DX-M1) SOM Board*.

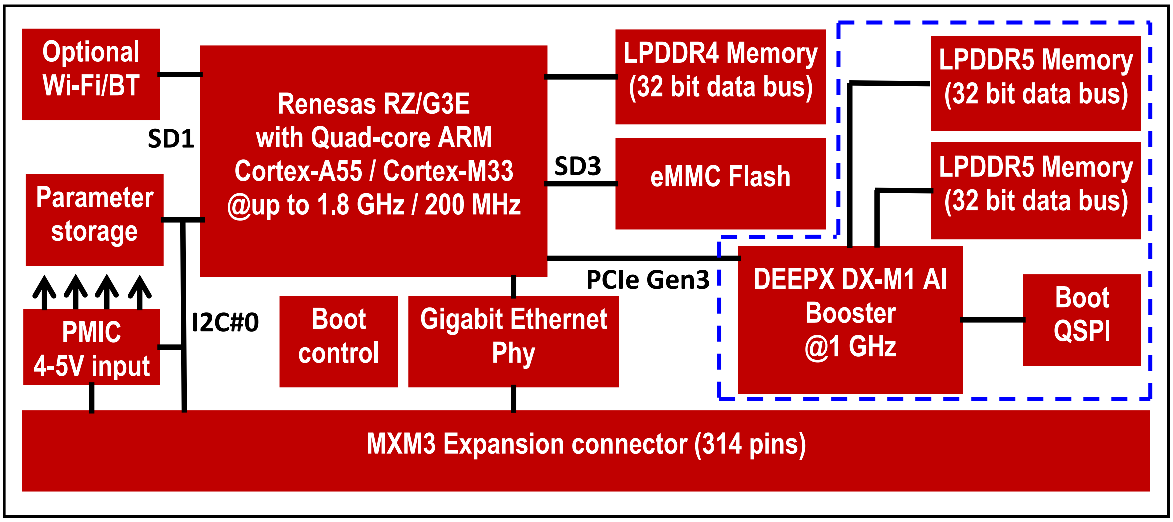


Figure 1 – RZ/G3E (DX-M1) SOM Board Block Diagram

The *RZ/G3E (DX-M1) SOM Board* pin assignment focuses on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four- or six-layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *SOM Boards* from Embedded Artists and the general, so called, EACOM specification is found in a separate document.

2.2 Software

The *RZ/G3E (DX-M1) SOM Board* has Board Support Packages (BSPs) for Embedded Linux. Precompiled images are available. Embedded Artists collaborate with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *RZ/G3E (DX-M1) SOM Board* for more information about software development.

2.3 Features and Functionality

The RZ/G3E is a powerful SoC. The full specification is found in Renesas' *RZ/G3E Group Datasheet* and *RZ/G3E Group User's Manual: Hardware*. The table below lists the key features and functions of the *RZ/G3E (DX-M1) SOM Board* - which represents Embedded Artists' integration of the RZ/G3E SoC. Due to pin configuration, some functions and interfaces of the RZ/G3E may not be available at the same time. See RZ/G3E SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature	RZ/G3E (DX-M1) SOM Board
CPUs	Renesas SoC commercial and industrial temp.	R9A09G047E57GBG (-40 - 85° C)
	CPU Cores	4x Cortex-A55 1x Cortex-M33
	L1 Instruction cache	32 KByte for each Cortex-A55 with parity
	L1 Data cache	32 KByte for each Cortex-A55 with ECC

	L2 Cache on Cortex-A55 cores	0 KByte
	L3 Cache on Cortex-A55 cores	1 MByte with ECC
	On-chip system SRAM	256 + 256 KByte with ECC
	NEON SIMD media accelerator on Cortex-A55	✓
	Maximum CPU frequency	1.8 GHz on Cortex-A55 cores 200 MHz on Cortex-M33
Security Functions	ARM TrustZone	✓
	Cryptographic Acceleration (RSIP-E50B)	✓
	SEC authentication of debug interface	✓
Memory	LPDDR4 RAM Size	1-4 GByte
	LPDDR4 RAM Speed	3200 MT/s
	LPDDR4 RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	8-256 GByte
Graphical Processing	3D Graphics Engine (GE3D)	Arm Mali-G52 630 MHz Vulkan 1.2, OpenCL 2.0, OpenGL ES 3.2/2.0/1.1
Video Processing	Video Codec Unit (VCD)	H.264/H.265 decode/encode 1080p60 H.264
	Frame Data Processor (FDP)	✓
	Video Signal Processor (VSP)	✓
Graphical Output	MIPI-DSI, 4 lanes	Up to 1920x1200px 60Hz resolution Pixel clk rate: 5.4 to 187.5 MHz
	Dual LVDS interfaces, supporting single and dual links	Up to 1920x1200px 60Hz resolution Pixel clk rate: LVDS (single) = 25 to 87 MHz LVDS (dual) = 50 to 174 MHz
	24-bit Parallel RGB interface	Up to 1280x800px 60Hz resolution Pixel clk rate: 5.4 to 187.5 MHz
Graphical Input	MIPI-CSI, 4 lanes	✓
Communication	Ethernet	Dual 1000/100/10 Mbps Gigabit Ethernet with support for IEEE1588. Dual on-board Gigabit PHY based on Microchip KSZ9131RNXI
	Wi-Fi/BT - optional	Optional Murata LBEE5HY2FY (2FY), 802.11a/b/g/n/ac/ax SISO, Wi-Fi 6E and 5.4 BR/EDR/BLE,

		SDIO interface, based on Infineon chipset CYW55513
NPU	Micro Neural network Processing Unit (NPU)	Arm Ethos-U55 1.0 GHz 256MAC, 0.5 TOPS
AI Booster	NPU - optional	DEEPX DX-M1 AI Booster, up to 25TOPS. Frequency up to 1 GHz
	SDRAM - optional	4GByte LPDDR5 5600MT/s, 64-bit/4ch databus
Connectivity Interfaces (all functions are not available at the same time)	USB3.2 Host Gen2	✓ up to 10Gbps
	USB2.0 OTG	✓
	USB2.0 Host	✓
	1x PCIe Gen3 (2 data lanes)	**Note:** Available if DX-M1 AI Booster not mounted. If the AI Booster is mounted, the PCIe interface is used to communicate with the DX-M1.
	6x CANFD	✓
	5/10-ch SSIU, 3-ch SPDIF, 6-ch PDM	✓
	2x SD3.0/MMC 5.0	✓ one interface used when on-board Wi-Fi/BT is mounted
	3x RSPI, 10x RSCI (UART), 9x I²C, 1x I³C	✓
	General PWM, WDT, General Timer, RTC	✓
	8x ADC	✓ 12bits
Other	PMIC supporting low power modes	✓
	E2PROM storing board information and Ethernet MAC addresses	✓
	On-board RTC via PMIC	✓
	On-board watchdog functionality	✓

2.4 Reference Documents

The following Renesas documents are also important reference documents and should be consulted for functional details:

- RZ/G3E Group Datasheet, latest revision
- RZ/G3E Group User's Manual: Hardware, latest revision
- RZ/G3E Product Mask Version Change (EPPO-EX-25-0028)
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- R01AN7542EJ0110, Power Consumption Measurement, latest revision
- R01AN7619EJ0100, Power Estimation Examples, latest revision

- R01AN7618EJ0100, Thermal Management Guideline, latest revision
- R01AN7546EJ0100, Lifetime Guideline, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now RENESAS) (www.Renesas.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now RENESAS) (www.Renesas.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has created the *EACOM Board Specification* that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the EACOM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the EACOM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

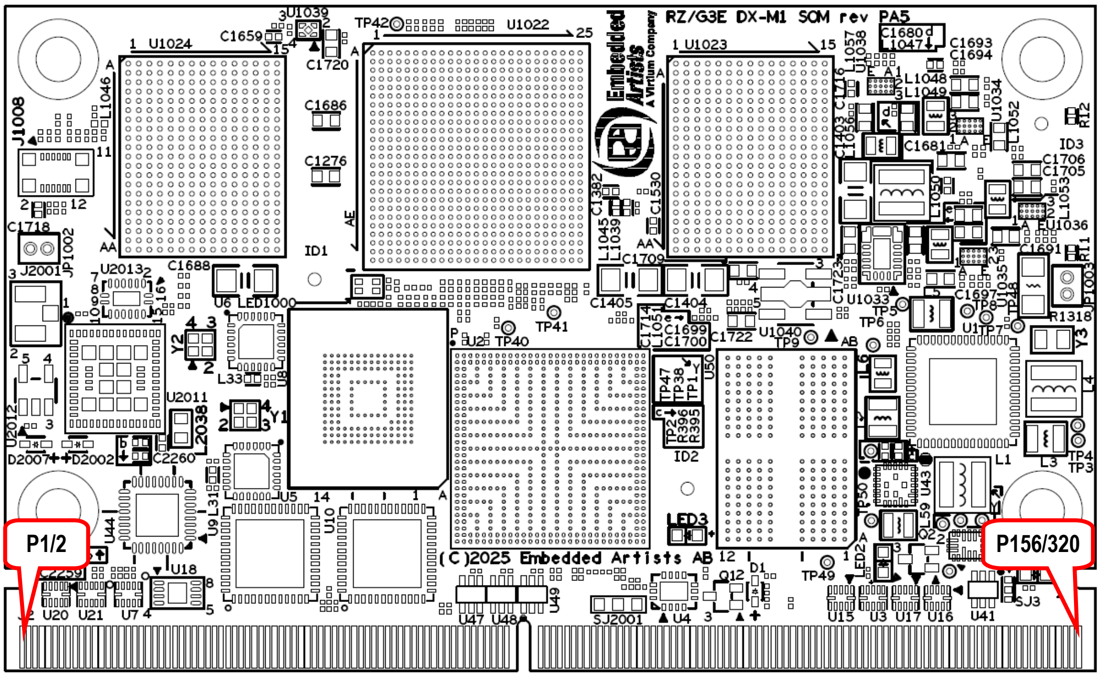


Figure 2 – EACOM Board Pin Numbering, Top Side

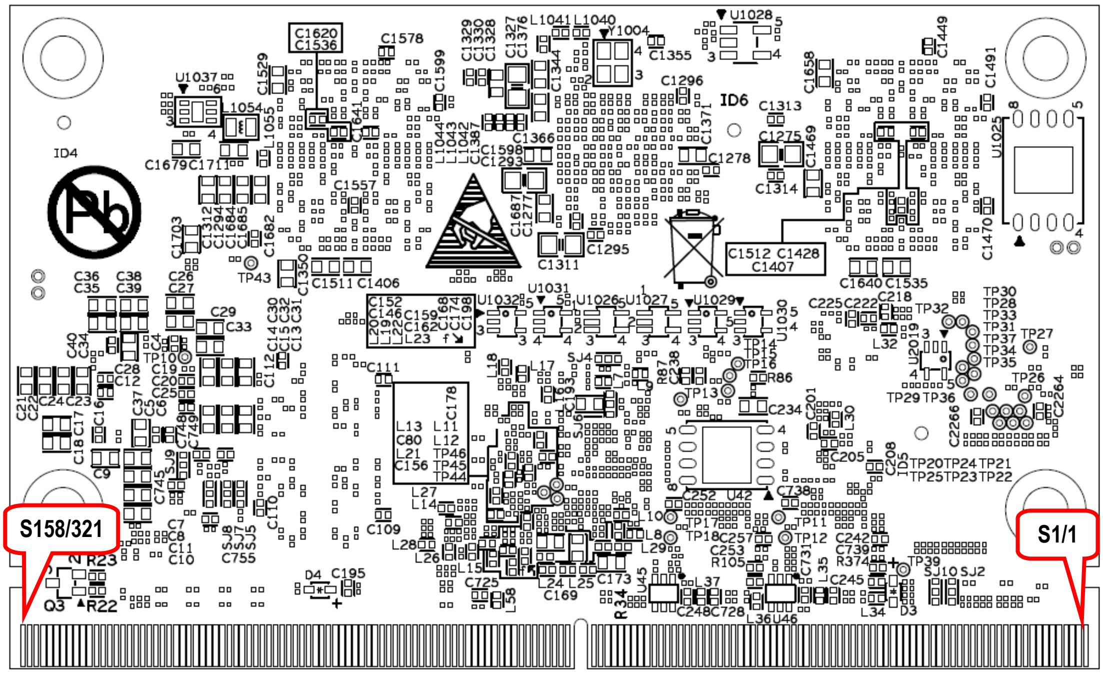


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different EACOM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
RZ/G3E Ball Name	The name of the RZ/G3E SoC ball (or other component on the EACOM board) that is connected to this pin.
Alternative Pin Function	Information if the signal is a dedicated interface or a general pin that can multiples different signals. See a separate Excel sheet for details about available multiplexing alternatives.
Signaling voltage	Information about the signaling voltage, if a general-purpose pin.
Notes	When relevant, the preferred pin function is listed.

There are 54 ground pins, which is about 17%, and 10 input supply voltage pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	RZ/G3E Ball Name	Alternative pin functions?	Signaling voltage	Notes
P1/2	GPIO-F	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_7
P2/4	GPIO-E	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_6
P3/6	GPIO-D	P14	Yes	3.3V	
P4/8	GPIO-C	P16	Yes	3.3V	
P5/10	SD_D1	PG3	Yes	1.8/3.3V	Controlled by alternative pin function SD1DAT1. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P6/12	SD_D0	PG2	Yes	1.8/3.3V	Controlled by alternative pin function SD1DAT0. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P7/14	SD_CLK	PG0	Yes	1.8/3.3V	Controlled by alternative pin function SD1CLK. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P8/16	SD_CMD	PG1	Yes	1.8/3.3V	Controlled by alternative pin function SD1CMD. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P9/18	SD_D3	PG5	Yes	1.8/3.3V	Controlled by alternative pin function SD1DAT3. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P10/20	SD_D2	PG4	Yes	1.8/3.3V	Controlled by alternative pin function SD1DAT2. **Note**: Logic level (3.3V or 1.8V) depends on NVCC_SD1, which is controlled by the Linux BSP via pin P15.
P11/22	SD_VCC				Not connected.
P12/24	MMC_D1	PH3	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2DAT1. **Note**: Logic level is fixed at 1.8V.
P13/26	MMC_D0	PH2	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2DAT0. **Note**: Logic level is fixed at 1.8V.
P14/28	MMC_D7				Not connected.
P15/30	MMC_D6				Not connected.
P16/32	MMC_CLK	PH0	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2CLK. **Note**: Logic level is fixed at 1.8V.
P17/34	MMC_D5				Not connected.
P18/36	MMC_CMD	PH1	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2CMD. **Note**: Logic level is fixed at 1.8V.

P19/38	MMC_D4				Not connected.
P20/40	MMC_D3	PH5	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2DAT3. **Note**: Logic level is fixed at 1.8V.
P21/42	MMC_D2	PH4	Yes	1.8V	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function SD2DAT2. **Note**: Logic level is fixed at 1.8V.
P22/44	GND				
P23/46	HDMI_TXC_N	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO2_5. **Note**: Non-standard pin allocation.
P24/48	HDMI_TXC_P	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO2_6. **Note**: Non-standard pin allocation.
P25/50	GND				
P26/52	HDMI_TXD0_N	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO2_7. **Note**: Non-standard pin allocation.
P27/54	HDMI_TXD0_P	SD0PWEN	Yes	1.8V	**Note**: Logic level is fixed at 1.8V. **Note**: Non-standard pin allocation.
P28/56	HDMI_HPD				Not connected
P29/58	HDMI_TXD1_N				Not connected
P30/60	HDMI_TXD1_P				Not connected
P31/62	GND				
P32/64	HDMI_TXD2_N				Not connected
P33/66	HDMI_TXD2_P				Not connected
P34/68	HDMI_CEC				Not connected
P35/70	GND				
P36/72	ETH1_MD1_P	ETH0_TRXP1	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 5
P37/74	ETH1_MD1_N	ETH0_TRXN1	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 6
P38/76	GND				
P39/78	ETH1_MD0_P	ETH0_TRXP0	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 2
P40/80	ETH1_MD0_N	ETH0_TRXN0	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 3
P41/82	ETH1_LINK1000	ETH0_LED1000	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 15 **Note**: ETH0_LED1000 and ETH0_LED100 are controlled by the same signal. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P42/84	ETH1_ACT	ETH0_LEDACT	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 17 via an open-drain buffer. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P43/86	ETH1_LINK	ETH0_LED100	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 15 **Note**: ETH0_LED100 and ETH0_LED1000 are controlled by the same signal. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P44/88	ETH1_MD3_N	ETH0_TRXN3	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 11
P45/90	ETH1_MD3_P	ETH0_TRXP3	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 10

P46/92	GND				
P47/94	ETH1_MD2_N	ETH0_TRXN2	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 8
P48/96	ETH1_MD2_P	ETH0_TRXP2	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 7
P49/98	GND				
P50/100	ETH2_MD1_P	ETH1_TRXP1	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 5
P51/102	ETH2_MD1_N	ETH1_TRXN1	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 6
P52/104	GND				
P53/106	ETH2_MD0_P	ETH1_TRXP0	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 2
P54/108	ETH2_MD0_N	ETH1_TRXN0	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 3
P55/110	ETH2_LINK1000	ETH1_LED1000	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 15 **Note**: ETH1_LED1000 and ETH1_LED100 are controlled by the same signal. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P56/112	ETH2_ACT	ETH1_LEDACT	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 17 via an open-drain buffer. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P57/114	ETH2_LINK	ETH1_LED100	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 15 **Note**: ETH1_LED100 and ETH1_LED1000 are controlled by the same signal. **Note**: The signal has a 10Kohm pull-up resistor to 3.3V.
P58/116	ETH2_MD3_N	ETH1_TRXN3	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 11
P59/118	ETH2_MD3_P	ETH1_TRXP3	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 10
P60/120	GND				
P61/122	ETH2_MD2_N	ETH1_TRXN2	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 8
P62/124	ETH2_MD2_P	ETH1_TRXP2	No		Connects to Ethernet-PHY KSZ9131RNXI, pin 7
P63/126	GND				
P64/128	USB_O1_DN	USB20_DN	No		
P65/130	USB_O1_DP	USB20_DP	No		
P66/132	USB_O1_OTG_ID	USB20_ID	No		
P67/134	USB_O1_SSTXN				Not connected
P68/136	USB_O1_SSTXP				Not connected
P69/138	GND				
P70/140	USB_O1_SSRXN				Not connected
P71/142	USB_O1_SSRXP				Not connected
P72/144	USB_O1_VBUS	USB20_VBUS	No		**Note**: This supply voltage must be connected to the USB20 interface to operate. The input is 5V tolerant.
P73/146	USB_O1_PWR_EN	P01	Yes	3.3V	Controlled by alternative pin function USB20_VBUSEN.
P74/148	USB_O1_OC	P00	Yes	3.3V	Controlled by alternative pin function USB20_OVRCURN.
150	Non existing pin				
152	Non existing pin				
154	Non existing pin				
156	Non existing pin				
P75/158	USB_H1_PWR_EN	P40	Yes	3.3V	Controlled by alternative pin function USB30_VBUSEN.
P76/160	USB_H1_OC	P41	Yes	3.3V	Controlled by alternative pin function

					USB30_OVRCURN.
P77/162	GND				
P78/164	USB_H1_DN	USB30_DN	No		
P79/166	USB_H1_DP	USB30_DP	No		
P80/168	USB_H1_SSTXN	USB30_TX0M	No		
P81/170	USB_H1_SSTXP	USB30_TX0P	No		
P82/172	GND				
P83/174	USB_H1_SSRXN	USB30_RX0M	No		
P84/176	USB_H1_SSRXP	USB30_RX0P	No		
P85/178	USB_H1_VBUS				Not connected **Note**: USB30 is Host-only.VBUS detect is not needed.
P86/180	USB_H2_PWR_EN	PK3	Yes	3.3V	Controlled by alternative pin function USB21_VBUSEN.
P87/182	USB_H2_OC	PG6	Yes	3.3V	Controlled by alternative pin function USB21_OVRCURN.
P88/184	GND				
P89/186	USB_H2_DN	USB21_DN	No		
P90/188	USB_H2_DP	USB21_DP	No		
P91/190	GND				
P92/192	COM board specific	NVCC_RF		3.3V	External power supply input to (optional) Wi-Fi/BT module. Not connected if no Wi-Fi/BT module is mounted.
P93/194	COM board specific	NVCC_RF		3.3V	External power supply input to (optional) Wi-Fi/BT module. Not connected if no Wi-Fi/BT module is mounted.
P94/196	COM board specific	GND			
P95/198	COM board specific	GND			
P96/200	COM board specific	NVCC_1V8		1.8V	1.8V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P97/202	COM board specific	NVCC_1V8		1.8V	1.8V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P98/204	COM board specific	GND			
P99/206	COM board specific	GND			
P100/208	COM board specific	NVCC_3V3		3.3V	3.3V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P101/210	COM board specific	NVCC_3V3		3.3V	3.3V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P102/212	COM board specific	GND			
P103/214	COM board specific	GND			
P104/216	COM board specific	BT_PCM_OUT	No	1.8V	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P105/218	COM board specific	BT_PCM_CLK	No	1.8V	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P106/220	COM board specific	BT_PCM_IN	No	1.8V	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic

P107/222	COM board specific	BT_PCM_SYNC	No	1.8V	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P108/224	COM board specific: M1_PWR_EN	PL7	No	1.8V	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. **Note:** Signal is 1.8V logic
P109/226	COM board specific: M1_PCIE_RST	PL6	No	1.8V	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. **Note:** Signal is 1.8V logic
P110/228	COM board specific: M1_PCIE_WAKE_N_OD	PL5	No	1.8V	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Signal is driven by the DX-M1. **Note:** Signal is 1.8V logic
P111/230	COM board specific: PCIE_CLKREQ_N_OD	PL4	No	1.8V	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Signal is driven by the DX-M1. **Note:** Signal is 1.8V logic
P112/232	COM board specific: HDMI_CECCLK	-	No	1.8V	Internal HDMI CEC clock, 12.0000MHz. Note: It is recommended to terminate this signal with a 50 ohm resistor to ground. Note that the voltage level is 1.8V.
P113/234	COM board specific: SLEEP#	-	No		This is an observation signal. It is pulled low (<0.4V when the system is in sleep more. Signal connects to the MPIO3 input, pin 2, on RAA215300A2GNP#HA8 PMIC. **Note**: Do not control this signal (pulling it high or low). The signal is driven internally by a push-pull driver.
P114/236	COM board specific: VIN_PWR_BAD#	-	No		Signal connects to the CEN input, pin 47, on RAA215300A2GNP#HA8 PMIC. This input signal can be pulled low (<0.4V) if the input supply voltage is outside of the valid range. **Note:** There is a 10 Kohm pull-up resistor to VIN on this signal.
P115/238	COM board specific: POWER_BTN#	-	No		Pull signal low (<0.4V) for two seconds to power-up the system. **Note:** There is a 10 Kohm pull-up resistor to VIN on this signal. **Note**: Signal is 5V tolerant.
P116/240	COM board specific	P21	Yes	1.8V	Controlled by alternative pin function I3C_SDA.
P117/242	COM board specific	P20	Yes	1.8V	Controlled by alternative pin function I3C_SCL.
P118/244	GND				
P119/246	SPI-B_SSEL	PM7	Yes, but output only	3.3V	Controlled by alternative pin function RSCI8_SSLA
P120/248	SPI-B_MOSI	PM5	Yes, but output only	3.3V	Controlled by alternative pin function RSCI8_MOSI
P121/250	SPI-B_MISO	PM4	Yes, but input only	3.3V	Controlled by alternative pin function RSCI8_MISO
P122/252	SPI-B_CLK	PM6	Yes, but	3.3V	Controlled by alternative pin function RSCI8_SCK

			output only		
P123/254	SPI-A_SSEL	P33	Yes, but output only	3.3V	Controlled by alternative pin function RSPI0_SSLA
P124/256	SPI-A_MOSI	P31	Yes, but output only	3.3V	Controlled by alternative pin function RSPI0_MOSI
P125/258	SPI-A_MISO	P30	Yes, but input only	3.3V	Controlled by alternative pin function RSPI0_MISO
P126/260	SPI-A_CLK	P32	Yes, but output only	3.3V	Controlled by alternative pin function RSPI0_RSPCKA
P127/262	GND				
P128/264	UART-C_RXD	PA4	Yes	3.3V	Controlled by alternative pin function RSCI7_RXD **Note:** Signal is typically used for Cortex-M console.
P129/266	UART-C_TXD	PA5	Yes	3.3V	Controlled by alternative pin function RSCI7_TXD **Note:** Signal is typically used for Cortex-M console.
P130/268	UART-B_RXD	P10	Yes		Controlled by alternative pin function RSCI2_RXD **Note:** Signal is typically used for Bluetooth module UART interface.
P131/270	UART-B_CTS	P13	Yes		Controlled by alternative pin function RSCI2_RTSN **Note:** Signal is typically used for Bluetooth module UART interface.
P132/272	UART-B_RTS	P12	Yes		Controlled by alternative pin function RSCI2_CTSN **Note:** Signal is typically used for Bluetooth module UART interface.
P133/274	UART-B_TXD	P11	Yes		Controlled by alternative pin function RSCI2_TXD **Note:** Signal is typically used for Bluetooth module UART interface.
P134/276	UART-A_RXD	SCIF_RXD	Yes, but input only	3.3V	**Note**: This signal is the receive input for serial bootloader mode. **Note:** Signal is typically used for the Linux console (Cortex-A).
P135/278	UART-A_CTS	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_2.
P136/280	UART-A_RTS	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_1.
P137/282	UART.A_TXD	SCIF_TXD	Yes, but output only	3.3V	**Note**: This signal is the transmit input for serial bootloader mode. **Note:** Signal is typically used for the Linux console (Cortex-A).
P138/284	PWM	PG7	Yes	3.3V	Controlled by alternative pin function GPT0_GTIOC5B
P139/286	GPIO-B	PK0	Yes	3.3V	Controlled by alternative pin function GPIO
P140/288	GPIO-A	P17	Yes	3.3V	Controlled by alternative pin function GPIO
P141/290	PERI_PWR_EN			3.3V	The output enable signal (active high) signals to the carrier board that peripheral can power up, i.e., signals to the SOM are allowed to be driven high. **Note: When this supply is logically high (3.3V), external circuitry that drives any MXM3 pin can also be powered.**
P142/292	RESET_IN	-	-		Reset input, active low. Pull signal low to activate reset. There is no need to pull signal high externally. There is a 10 Kohm pull-up resistor to VIN on this signal. The input is 5V tolerant.
P143/294	RESET_OUT				Reset (open drain) output, active low. Driven low during reset. There is no (on-board) pull-up resistor. An external pull-up resistor is needed with minimum value of 1 Kohm.

					The supply voltage to connect to can be anywhere between 1.8 to 5V.
P144/296	VIN_SELECT				This output is connected to VIN via a 1Kohm resistor to signal that supply voltage VIN shall be 3.5-5V. This signal can be used by carrier boards that can support EACOM boards that require 3.3V on VIN (in this case, this pin is connected to ground). If only the SOM board family shall be supported, which is the normal case, ignore this pin and do not connect to it.
P145/298	VBAT_RTC				Signal connects to the VBAT input, pin 30, on the RAA215300A2GNP#HA8 PMIC. Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	ISP_ENABLE				Control the boot mode of the RZ/G3E SoC. See chapter 6 for details. Should be left open for normal operation (will write protect the on-board parameter storage E2PROM) or connected to GND (will enable write to the on-board parameter storage E2PROM). **Note**: Signal has a 100 Kohm pull-up resistor to 1.8V.
P147/302	VIN				Main input voltage supply (3.5-5V)
P148/304	VIN				Main input voltage supply (3.5-5V)
P149/306	VIN				Main input voltage supply (3.5-5V)
P150/308	VIN				Main input voltage supply (3.5-5V)
P151/310	VIN				Main input voltage supply (3.5-5V)
P152/312	VIN				Main input voltage supply (3.5-5V)
P153/314	VIN				Main input voltage supply (3.5-5V)
P154/316	VIN				Main input voltage supply (3.5-5V)
P155/318	VIN				Main input voltage supply (3.5-5V)
P156/320	VIN				Main input voltage supply (3.5-5V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	RZ/G3E Ball Name	Alternative pin functions?	Signaling voltage	Notes
S1/1	MQS_RIGHT	P07	Yes	3.3V	Controlled by alternative pin function SSI4_WS
S2/3	MQS_LEFT	P06	Yes	3.3V	Controlled by alternative pin function SSI4_SCK
S3/5	GND				
S4/7	AUDIO_TXFS	P04	Yes	3.3V	Controlled by alternative pin function SSI3_WS
S5/9	AUDIO_RXD	P05	Yes	3.3V	Controlled by alternative pin function SSI4_SDATA
S6/11	AUDIO_TXC	P03	Yes	3.3V	Controlled by alternative pin function SSI3_SCK
S7/13	AUDIO_TXD	P02	Yes	3.3V	Controlled by alternative pin function SSI3_SDATA
S8/15	AUDIO_MCLK	AUDIO_MCLK	Yes	3.3V	Internal audio bit clock, 11.2896MHz or 12.2880MHz. Frequency controlled by Linux BSP.
S9/17	GND				
S10/19	SPDIF_IN	PD4	Yes	Yes	Controlled by alternative pin function SPDIF2_IN
S11/21	SPDIF_OUT	PD5	Yes	Yes	Controlled by alternative pin function SPDIF2_OUT
S12/23	CAN2_TX	PD7	Yes	Yes	Controlled by alternative pin function CAN1_CTX

S13/25	CAN2_RX	PD6	Yes	Yes	Controlled by alternative pin function CAN1_CRX
S14/27	CAN1_TX	P45	Yes	Yes	Controlled by alternative pin function CANFD5_CTX
S15/29	CAN1_RX	P44	Yes	Yes	Controlled by alternative pin function CANFD5_CRX
S16/31	GND				
S17/33	LVDS1_D3_P	LVDS1_TX3_P			
S18/35	LVDS1_D3_N	LVDS1_TX3_N			
S19/37	GPIO-J	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_5.
S20/39	LVDS1_D2_P	LVDS1_TX2_P			
S21/41	LVDS1_D2_N	LVDS1_TX2_N			
S22/43	GND				
S23/45	LVDS1_D1_P	LVDS1_TX1_P			
S24/47	LVDS1_D1_N	LVDS1_TX1_N			
S25/49	GND				
S26/51	LVDS1_D0_P	LVDS1_TX0_P			
S27/53	LVDS1_D0_N	LVDS1_ TX0_N			
S28/55	GND				
S29/57	LVDS1_CLK_P	LVDS1_CLK_P			
S30/59	LVDS1_CLK_N	LVDS1_CLK_N			
S31/61	GND				
S32/63	LVDS0_D3_P	LVDS0_TX3_P			
S33/65	LVDS0_D3_N	LVDS0_TX3_N			
S34/67	GPIO-H	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_4.
S35/69	LVDS0_D2_P	LVDS0_TX2_P			
S36/71	LVDS0_D2_N	LVDS0_TX2_N			
S37/73	GND				
S38/75	LVDS0_D1_P	LVDS0_TX1_P			
S39/77	LVDS0_D1_N	LVDS0_TX1_N			
S40/79	GND				
S41/81	LVDS0_D0_P	LVDS0_TX0_P			
S42/83	LVDS0_D0_N	LVDS0_ TX0_N			
S43/85	GND				
S44/87	LVDS0_CLK_P	LVDS0_CLK_P			
S45/89	LVDS0_CLK_N	LVDS0_CLK_N			
S46/91	I2C-A_SDA	P35	No	3.3V	Controlled by alternative pin function RIIC2_SDA. Signal must be RIIC2_SDA since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S47/93	I2C-A_SCL	P34	No	3.3V	Controlled by alternative pin function RIIC2_SCL. Signal must be RIIC2_SCL since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S48/95	I2C-B_SDA	P37	No	3.3V	Controlled by alternative pin function RIIC3_SDA **Note**: This signal has as 2.2Kohm pullup resistor to an

					internally generated 3.3V supply.
S49/97	I2C-B_SCL	P36	No	3.3V	Controlled by alternative pin function RIIC3_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S50/99	HDMI/I2C-C_SDA	PL3	Yes	3.3V	Controlled by alternative pin function RIIC1_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S51/101	HDMI/I2C-C_SCL	PL2	Yes	3.3V	Controlled by alternative pin function RIIC1_SDA **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S52/103	TP_RST	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_3.
S53/105	TP_IRQ	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_2.
S54/107	DISP_PWR_EN	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_1.
S55/109	BL_PWR_EN	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO0_0.
S56/111	BL_PWM	PA6	Yes	3.3V	Controlled by alternative pin function GPT1_GTIOC12A
S57/113	GND				
S58/115	LCD_R0	P85	Yes	3.3V	Controlled by alternative pin function LCDC1_R0
S59/117	LCD_R1	P82	Yes	3.3V	Controlled by alternative pin function LCDC1_R1
S60/119	LCD_R2	P77	Yes	3.3V	Controlled by alternative pin function LCDC1_R2
S61/121	LCD_R3	P74	Yes	3.3V	Controlled by alternative pin function LCDC1_R3
S62/123	LCD_R4	P71	Yes	3.3V	Controlled by alternative pin function LCDC1_R4
S63/125	LCD_R5	P65	Yes	3.3V	Controlled by alternative pin function LCDC1_R5
S64/127	LCD_R6	P62	Yes	3.3V	Controlled by alternative pin function LCDC1_R6
S65/129	LCD_R7	P56	Yes	3.3V	Controlled by alternative pin function LCDC1_R7
S66/131	LCD_G0	P83	Yes	3.3V	Controlled by alternative pin function LCDC1_G0
S67/133	LCD_G1	P80	Yes	3.3V	Controlled by alternative pin function LCDC1_G1
S68/135	LCD_G2	P75	Yes	3.3V	Controlled by alternative pin function LCDC1_G2
S69/137	LCD_G3	P72	Yes	3.3V	Controlled by alternative pin function LCDC1_G3
S70/139	LCD_G4	P66	Yes	3.3V	Controlled by alternative pin function LCDC1_G4
S71/141	LCD_G5	P63	Yes	3.3V	Controlled by alternative pin function LCDC1_G5
S72/143	LCD_G6	P60	Yes	3.3V	Controlled by alternative pin function LCDC1_G6
S73/145	LCD_G7	P54	Yes	3.3V	Controlled by alternative pin function LCDC1_G7
S74/147	GND			3.3V	
S75/149	LCD_B0	P84	Yes	3.3V	Controlled by alternative pin function LCDC1_B0
151	Non existing pin				
153	Non existing pin				
155	Non existing pin				
S76/157	LCD_B1	P81	Yes	3.3V	Controlled by alternative pin function LCDC1_B1
S77/159	LCD_B2	P76	Yes	3.3V	Controlled by alternative pin function LCDC1_B2
S78/161	LCD_B3	P73	Yes	3.3V	Controlled by alternative pin function LCDC1_B3
S79/163	LCD_B4	P70	Yes	3.3V	Controlled by alternative pin function LCDC1_B4
S80/165	LCD_B5	P64	Yes	3.3V	Controlled by alternative pin function LCDC1_B5
S81/167	LCD_B6	P61	Yes	3.3V	Controlled by alternative pin function LCDC1_B6
S82/169	LCD_B7	P55	Yes	3.3V	Controlled by alternative pin function LCDC1_B7

S83/171	LCD_CLK	P50	Yes	3.3V	Controlled by alternative pin function LCDC1_CLK
S84/173	GPIO-G	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_0.
S85/175	LCD_HSYNC	P51	Yes	3.3V	Controlled by alternative pin function LCDC1_HSYNC
S86/177	LCD_VSYNC	P52	Yes	3.3V	Controlled by alternative pin function LCDC1_VSYNC
S87/179	LCD_ENABLE	P53	Yes	3.3V	Controlled by alternative pin function LCDC1_DE
S88/181	GND				
S89/183	AIN_VREF			1.8V	Connected to an internal 1.8V power supply that is always on.
S90/185	AIN7	AINI007	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S91/187	AIN6	AINI006	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S92/189	AIN5	AINI005	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S93/191	AIN4	AINI004	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S94/193	AIN3	AINI003	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S95/195	AIN2	AINI002	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S96/197	AIN1	AINI001	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S97/199	AIN0	AINI000	No, ADCIN only	1.8V	Note that maximum input voltage is 1.8V
S98/201	GND				
S99/203	COM board specific	DSI_DNDATA0	No		
S100/205	COM board specific	DSI_DPDATA0	No		
S101/207	GND				
S102/209	COM board specific	DSI_DNDATA1	No		
S103/211	COM board specific	DSI_DPDATA1	No		
S104/213	GND				
S105/215	COM board specific	DSI_DNCLK	No		
S106/217	COM board specific	DSI_DPCLK	No		
S107/219	COM board specific	GND			
S108/221	COM board specific	DSI_DNDATA2	No		
S109/223	COM board specific	DSI_DPDATA2	No		
S110/225	COM board specific	GND			
S111/227	COM board specific	DSI_DNDATA3	No		
S112/229	COM board specific	DSI_DPDATA3	No		

S113/231	COM board specific	GND			
S114/233	CSI_HSYNC	QRESN	No	1.8V	Signal connects directly to the QRESN input on the RZ/G3E SoC. **Note:** Signal is 1.8V logic and has a 10Kohm pull-up resistor to an internally generated 1.8V supply (1V8_AWO). This signal should only be driven low. This signal is used for a debug interface system reset. **Note**: Non-standard pin allocation.
S115/235	CSI_VSYNC	PJ4	Yes	1.8V	Controlled by alternative pin function JTAG_TRST. **Note:** Signal is 1.8V logic. **Note**: Non-standard pin allocation.
S116/237	CSI_MCLK	PJ2	Yes	1.8V	Controlled by alternative pin function JTAG_TDO. **Note:** Signal is 1.8V logic. **Note**: Non-standard pin allocation.
S117/239	CSI_PCLK	PJ3	Yes	1.8V	Controlled by alternative pin function JTAG_TDI. **Note:** Signal is 1.8V logic. **Note**: Non-standard pin allocation.
S118/241	GND				
S119/243	CSI_D0	PJ0	Yes	1.8V	Controlled by alternative pin function JTAG_TMS/SWDIO. **Note:** Signal is 1.8V logic. **Note**: Non-standard pin allocation.
S120/245	CSI_D1	PJ1	Yes	1.8V	Controlled by alternative pin function JTAG_TCK/SWCLK. **Note:** Signal is 1.8V logic. **Note**: Non-standard pin allocation.
S121/247	CSI_D2	-	-	1.8V	Connected to the internally generated 1.8V power supply. This is the signaling voltage of the JTAG interface. **Note**: Non-standard pin allocation.
S122/249	CSI_D3	MD_BOOT3	No	1.8V	Pull signal low to disable the JTAG/SWD debug interface. **Note**: Signal has a 10Kohm pull-up resistor to 1.8V
S123/251	CSI_D4	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_6. **Note**: Non-standard pin allocation.
S124/253	CSI_D5	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_5. **Note**: Non-standard pin allocation.
S125/255	CSI_D6	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_4. **Note**: Non-standard pin allocation.
S126/257	CSI_D7	-	Only GPIO	3.3V	Connected to I2C-A GPIO-expander, IO1_3. **Note**: Non-standard pin allocation.
S127/259	GND				
S128/261	CSI_D3_M	CSI0_DATA3N	No	No	
S129/263	CSI_D3_P	CSI0_DATA3P	No	No	
S130/265	GND				
S131/267	CSI_D2_M	CSI0_DATA2N	No	No	

S132/269	CSI_D2_P	CSI0_DATA2P	No	No	
S133/271	GND				
S134/273	CSI_D1_M	CSI0_DATA1N	No	No	
S135/275	CSI_D1_P	CSI0_DATA1P	No	No	
S136/277	GND				
S137/279	CSI_D0_M	CSI0_DATA0N	No	No	
S138/281	CSI_D0_P	CSI0_DATA0P	No	No	
S139/283	GND				
S140/285	CSI_CLK_M	CSI0_CLKN	No	No	
S141/287	CSI_CLK_P	CSI0_CLKP	No	No	
S142/289	GND				
S143/291	PCIE_TX_P1	PCIE_TXDPL1	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S144/293	PCIE_TX_N1	PCIE_TXDNL1	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S145/295	GND				
S146/297	PCIE_RX_P1	PCIE_RXDPL1	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input
S147/299	PCIE_RX_N1	PCIE_RXDNL1	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input
S148/301	BOOT_CTRL		No	No	Control the boot mode of the RZ/G3E SoC. See chapter 6 for details. Signal should either be left open or connected to GND. **Note**: Signal has a 100 Kohm pull-up resistor to 1.8V.
S149/303	GND				
S150/305	PCIE_CLK_P	PCIE_REFCLKP0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: 100MHz PCIe reference clock output. The signals require a 50 ohm termination resistor to ground at the receiver end.
S151/307	PCIE_CLK_N	PCIE_REFCLKN0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: 100MHz PCIe reference clock output. The signals require a 50 ohm termination resistor to ground at the receiver end.
S152/309	GND				
S153/311	PCIE_TX_P0	PCIE_TXDPL0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S154/313	PCIE_TX_N0	PCIE_TXDNL0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S155/315	GND				
S156/317	PCIE_RX_P0	PCIE_RXDPL0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input
S157/319	PCIE_RX_N0	PCIE_RXDNL0	No	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input

S158/321	GND

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

An external pin of the RZ/G3E SoC is either a dedicated pin or a generic GPIO pin that have multiplexed functions (multiplexed pins). The PFC (Pin Function Controller) controls selection from among the multiplexed functions or of operation as general-purpose I/O (GPIO) port pins. This leaves great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

The dedicated pins have fixed functionality. These are typically interfaces with specific voltage levels/drivers/transceivers, like PCIe, LVDS, MIPI-DSI, MIPI-CSI and USB.

To keep compatibility between EACOM boards, the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *RZ/G3E (DX-M1) SOM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. For more information about the register settings, see the document: *RZ/G3E Group User's Manual: Hardware* from Renesas. Specifically see section *4.2 Pin Function Controller (PFC)* for details on how to control the functionality for each programmable pin. Normally this is controlled via the bootloader and Linux DTS file.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. There can be up to 15 different functions for each pin. The reset state is shown as well as the EACOM function allocation.

4.2 I/O Pin Control

Each pin also has additional control registers for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength, slew rate and more. Also in this case, configuration is normally done via the Linux BSP. For more information about the register settings, see the document: *RZ/G3E Group User's Manual: Hardware* from Renesas. Specifically see section *4.2 Pin Function Controller (PFC)* for details.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, some with pull-down resistor, some without, and some with pull-up resistor, after reset. Some pins are configured as Hi-Z outputs. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

The **RZ/G3E datasheet and reference manuals from Renesas shall always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously. There is an accompanying Excel document that lists all alternative functions for each available I/O pin. It is recommended to study this document to get an overview of the available pin multiplexing options.

The process of defining the pin/function for a system is:

1. Define which interfaces are needed in the system.
2. Allocate each needed interface to either Cortex-A55 ("Linux side") or M33 side ("real-time side").
3. Consult the Excel sheet and allocate the interfaces to different pins.
    a. If possible, follow the EACOM pin and interface allocation. It is not strictly needed but will simplify if the SOM board will be replaced in a future update/upgrade.
    b. Note that connector JC (and signals allocated to this connector) will not exist if on-board Wi-Fi/BT module is mounted.
    c. Note that not all signals have 3.3V logic level. Some also have 1.8V logic level.
4. When a suitable pin/function allocation has been done, update the *.dts file under Linux to enable the interfaces that shall be controlled from the A55/Linux side. On the M33 side, peripherals are enabled and initialized via function calls, see the SDK for details.
    a. If pin/function allocation is impossible, the basic architecture under 1) must be reexamined and updated.

6 Boot Control

This chapter presents the different boot settings that the *RZ/G3E (DX-M1) SOM Board* supports.

Note that this chapter only presents how the different options are controlled. If does not discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *RZ/G3E (DX-M1) SOM Board* supports booting (i.e., from where the RZ/G3E SoC starts downloading code to start executing from) from different sources:

1. On-board QSPI and external uSD memory card, **which is the current default to Q2-2026.**
2. On-board QSPI and eMMC Flash, **which will be the default after Q2-2026.**
3. SCIF Serial download (also called 'serial download' or "Recovery" mode).
4. USB download. This mode is an alternative to SCIF serial download, but as of Q2-2026 it is currently not supported.

Two signals control the booting source/process, BOOT_CTRL and ISP_ENABLE, see table below.

Note that in all cases, it is the Cortex-A55 cores that will boot. The RZ/G3E SoC can also start booting with the Cortex-M33 core, but that is not supported by default. For volume customers, it is possible to create custom versions that support Cortex-M33 booting.

Boot source	BOOT_CTRL	ISP_ENABLE
On-board QSPI + external uSD memory card The Cortex-A55 cores initially boots from the QSPI flash and then loads the Linux kernel and root file system from an external uSD memory card. **This is the default solution to Q2-2026.**	Floating Jumper open on carrier board	Floating Jumper open on carrier board
On-board eMMC The Cortex-A55 cores boots from the Linux kernel and root file system from the on-board eMMC. **This will be the default solution after Q2-2026.**	Low (grounded) Jumper inserted/shorted on carrier board	Floating Jumper open on carrier board
SCIF Serial download This is known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation.	Floating Jumper open on carrier board	Low (grounded) Jumper inserted/shorted on carrier board
USB download This is also known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation. **As of Q2-2026 it is currently not supported.**	Low (grounded) Jumper inserted/shorted on carrier board	Low (grounded) Jumper inserted/shorted on carrier board

On a custom carrier board, it is recommended to connect signal BOOT_CTRL to the ground via a zero-ohm resistor. Never directly connected to ground. This makes it easy to control the state of the pin (floating or grounded).

6.1 SOM Carrier Board Boot Control Jumpers

The picture below describes where to find the two boot control jumpers on the SOM Carrier Board.

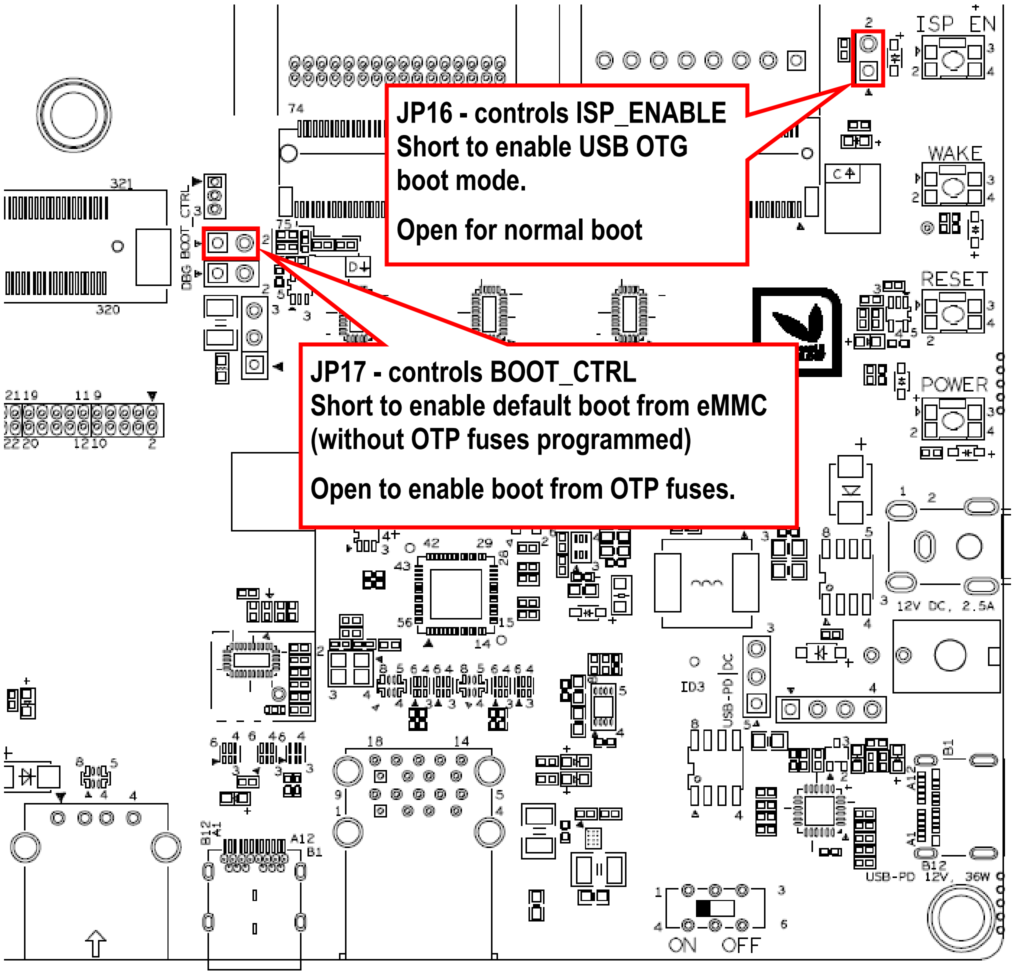


Figure 4 – SOM Carrier Board rev A, Boot Control Jumpers

7 Powering and PMIC Integration

The RZ/G3E SoC is tightly integrated with the PMIC (RAA215300A2GNP#HA8) to achieve high-performance and low-power operation of the *RZ/G3E (DX-M1) SOM Board*. The RAA215300A2GNP#HA8 PMIC is specifically developed for the RZ/G3E SoC. It also includes a real-time clock. See the RAA215300A2GNP#HA8 datasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are available for the carrier board design, reducing integration costs. Designs with moderate power consumption may not need any external power supply at all. Everything can be handled by the on-board PMIC. Section 7.1 presents the available power rails.

7.1 Available Power Supply Rails

The table below presents the available power rails that can be used on the carrier board that the *RZ/G3E (DX-M1) SOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
NVCC_3V3 **on MXM3 pins P100/208 and P101/210**	3.3V for external use.	3.3V	500mA
NVCC_1V8 **on MXM3 pins P96/200 and P97/202**	1.8V for external use.	1.8V	500mA

For any of above supply next, connect to both MXM3 pins, respectively, on the expansion connector that carry a specific power rail.

Note that external load variations can affect the PMIC operation and potentially disturb the RZ/G3E SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails. Also **calculate the heat dissipation** of the PMIC in case the carrier board has high current consumption.

8 Technical Specification

8.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.4	5.5	V
VBAT	RTC supply voltage	-0.4	5.5	V
VIO	Vin/Vout: 3.3V IO	-0.4	3.45	V
	Vin/Vout: 1.8V IO	-0.4	2.0	V
VADC	Voltage to ADC input	0	1.8	V
USB_xx_VBUS	USB VBUS signals	-0.4	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.4	3.63	V

8.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.5	5.0	5.5 50 10	V mV mV
VBAT	RTC supply voltage **Note:** This voltage must always remain valid for correct operation of the board (including, but not limited to the RTC).	1.8		5.5	V
USB_xx_VBUS	USB VBUS signals		5	5.25	V

8.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach the recommended operating range in 2-20 ms.

8.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see *RZ/G3E Group Datasheet*. The internal VDD operating point for GPIOs is 3.3V or 1.8V for all signals.

Specific high-speed interfaces, like MIPI, PCIe and LVDS have other operating voltages.

8.4.1 Reset Output Voltage Range

The reset output is an open drain output with no pull-up resistor. An external pull-up resistor is needed with minimum value of 1 Kohm. The supply voltage to connect to can be anywhere between 1.8 to 5V. Maximum output voltage when active is 0.4V.

8.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 100 mS minimum. The internal reset pulse will be about 10 mS long, before the RZ/G3E boot process starts.

8.5 Power Consumption

There are several factors that determine power consumption of the *RZ/G3E (DX-M1) SOM Board*, like input voltage, operating temperature, LPDDR4 activity, operating frequencies for the different cores and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

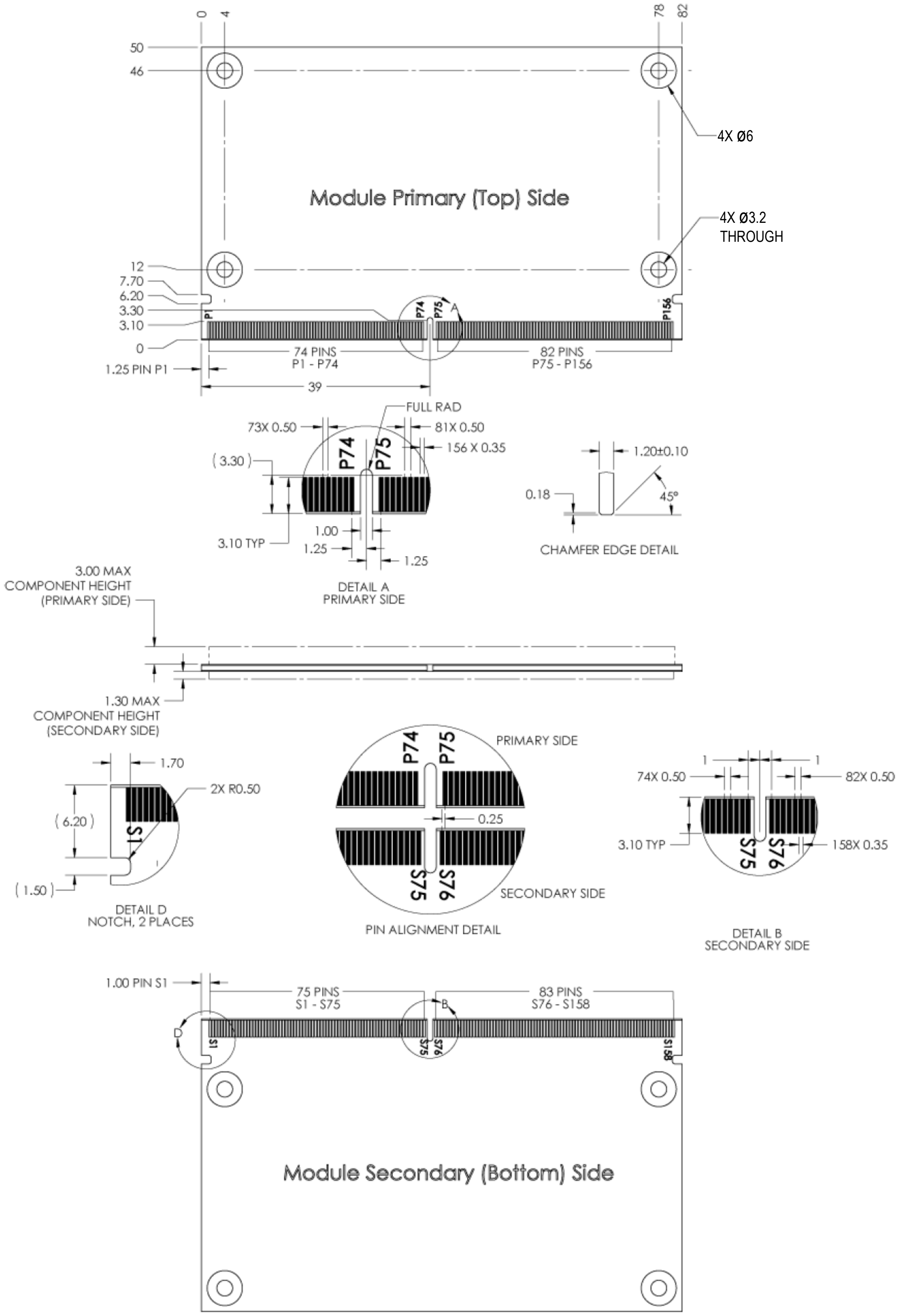
Symbol	Description (VIN = 5V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 1.8 GHz ARM frequency, without Ethernet		1000	mA
I_{VIN}_MAX_DX-M1	Maximum DX-M1 load, 1 GHz DX-M1 frequency Maximum CPU load, 1.8 GHz ARM frequency, without Ethernet		2100	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		130 TBD TBD	mA
I_{VIN}_LP	Low-power mode, aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA

8.6 Mechanical Dimensions

The board uses the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm
Module weight	16 ±7 gram	gram

The picture below illustrates the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and illustrates pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 5 – RZ/G3E (DX-M1) SOM Board Mechanical Outline

8.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers, at different board-to-board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE should not be used since this specific connector lacks some of the pins. It is, however, possible to use the connector if it is acceptable for the project not to use the following pins:

- P146/300 ISP_ENABLE This pin is also used to select USB OTG as boot mode (when pulled low), also known as "factory recovery" mode. Not having access to this pin means that USB OTG mode cannot be enabled from the carrier board.
- P147/302 VIN This is not a problem since there are many VIN pins.
- S149/303 GND This is not a problem since there are many GND pins.
- S148/301 GND This is not a problem since there are many GND pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the SOM Carrier board. This connector gives a board-to-board stacking height of 5.0 mm. This space allows some components to also be placed right under the SOM board.

Always check available component height before placing components on the carrier board under the SOM board, see picture below.

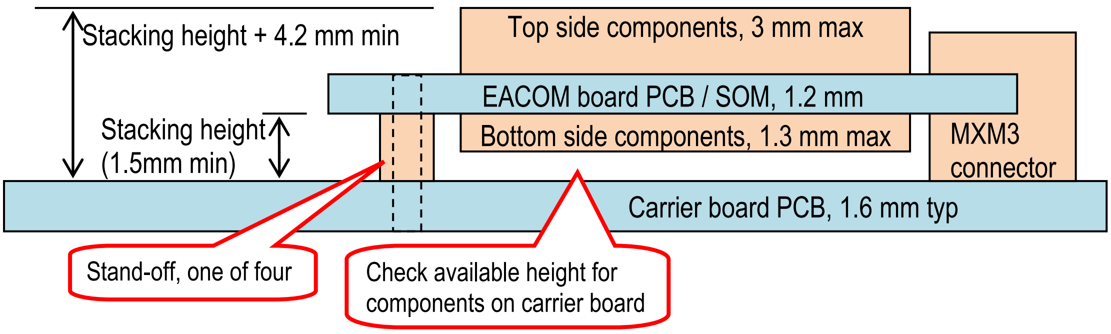


Figure 6 – SOM Board Mounting in MXM3 Connector, Stacking Height

8.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

Do not apply too high torque on the screws. That will create mechanical stress on the PCB and result on cracked BGA balls and/or cracked copper tracks. The order the screws are mounted and tightened is also very important. Do not tighten the screws immediately. Read the information in section 10.1 for details, including watching the YouTube video referred to.

8.7 Environmental Specification

8.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature RZ/G3E SoC, operating	comm. temp. range ind. temp. range.	0 -40	95 105	°C °C

[1] Depends on cooling/heat management solution.

8.7.2 Relative Humidity (RH)

Parameter		Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 70°C, non-condensing Operating: -40°C ≤ T_A ≤ 85°C, non-condensing	(comm. temp. range) (ind. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing		5	90	%

8.8 Thermal Design Considerations

Heat dissipation from the RZ/G3E SoC depends on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat can be up to 3 Watt but is typically much lower.

Whether external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *RZ/G3E (DX-M1) SOM Board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the RZ/G3E SoC.

The RZ/G3E SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affects several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: RZ/G3E Dual Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

External cooling is likely needed – more information about this will be added in a future revision of the document, including information about the DX-M1 thermal management.

Be very careful when mounting the heat sink. Do not apply force so that the PCB will bend. That will result in immediate failure of boards or long-term reliability problems.

8.8.1 Thermal Parameters

The RZ/G3E SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	14.8	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	0.38	°C/W

8.9 Product Compliance

Visit Embedded Artists' website at https://www.embeddedartists.com/product_compliance for up-to-date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

9 Functional Verification and RMA

There is a separate document that presents several functional tests that can be performed on the *RZ/G3E (DX-M1) SOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *RZ/G3E DX-M1 AI Kit* and *RZ/G3E Developer's Kit* together with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

10 Things to Note

This chapter presents a few issues and considerations that users must note.

10.1 Handle the SOM Board with Great Care

Handle the *RZ/G3E (DX-M1) SOM Board* with great mechanical care. Only remove/unmount it from the *SOM Carrier board* if absolutely needed. Watch the YouTube video we have published about this topic: https://www.youtube.com/watch?v=6mvVnA3Chbw, title "How to mount and unmount a COM board". Note that in this context, we use the term SOM and COM interchangeable. Even though the video refers to COM boards, the exact same handling principles apply to our SOM boards.

10.2 Shared Pins and Multiplexing

The RZ/G3E SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *RZ/G3E DX-M1 SOM* on-board design. Check if the interfaces needed are available to allocation before starting a design. See chapter 4 for details.

10.3 Only Use EA Board Support Package (BSP)

The *RZ/G3E (DX-M1) SOM Board* uses multiple on-board interfaces in the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace RZ/G3E (DX-M1) SOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

10.4 Boot Partition Size in eMMC

The size of the boot partition varies between different eMMC parts. The boot partition on parts mounted on the *RZ/G3E (DX-M1) SOM Board* will be 4 MByte minimum. It can be larger but never assume it is larger than 4 MByte. Design your system to only require 4 MByte to operate correctly.

10.5 OTP Fuse Programming

The RZ/G3E SoC has on-chip OTP fuses that can be programmed, see Renesas documents for details. Once programmed, there is no possibility of reprograming them.

RZ/G3E (DX-M1) SOM Boards are delivered without any OTP fuse programming. It is completely up to the SOM board user to decide if OTP fuses shall be programmed and, in that case, which ones.

Note that Embedded Artists does not replace RZ/G3E (DX-M1) SOM Boards because of wrong OTP programming. It's the user's responsibility to be certain before OTP programming and not to program the fuses by accident.

10.6 Write Protect on Parameter Storage E2PROM

There is an on-board I2C-E2PROM connected to I2C-channel #1 with 7-bit address 0x55 (8-bit address 0xAA/0xAB). The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write-protected if signal ISP_ENABLE (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the RZ/G3E SoC will boot into *SCIF or USB Download* mode (depending on the state of the BOOT_CTRL pin. Both these download modes are also called 'serial download' or 'factory recovery' modes.

Note that it is not possible to connect an external I2C-device to IC2-channel #1 on the carrier board with this address (since this address is taken by the on-board parameter storage memory).

10.7 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *RZ/G3E (DX-M1) SOM Board* targets a wide range of applications, such as:

- Edge Compute applications
- Edge AI applications
- HMI/GUI solutions
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *RZ/G3E (DX-M1) SOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If you have an application in this area, contact Embedded Artists for a discussion.

If not before, **it is essential to contact Embedded Artists before production begins**. To ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *RZ/G3E (DX-M1) SOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *RZ/G3E (DX-M1) SOM Board*.

10.8 ESD Precaution when handling RZ/G3E (DX-M1) SOM Board

Please note that the *RZ/G3E (DX-M1) SOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel should handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the board to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

10.9 EMC / ESD

The *RZ/G3E (DX-M1) SOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless, depending on the target system, additional anti-interference measures may still be necessary to adhere to the limits for the overall system.

The *RZ/G3E (DX-M1) SOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only make sense of the complete solution.

No specific ESD protection has been implemented on the *RZ/G3E (DX-M1) SOM Board*. ESD protection on board level is the same as what is specified in the RZ/G3E SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs and outputs of the system.

11 Custom Design

This document specifies the standard *RZ/G3E (DX-M1) SOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Mounting a different Wi-Fi/BT module.
- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different board form factors, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are taller (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *RZ/G3E (DX-M1) SOM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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Customer is required to take note of manufacturer's specification of used components, for example PMIC and eMMC. Such specifications, if applicable, contain additional information that must be taken note of for the safe and reliable operation. These documents are stored on Embedded Artists' product support page.

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