iMX8M Mini DX-M1 SOM Datasheet

Get Up-and-Running Quickly and
Start Developing Your Application On Day 1!

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1 Document Revision History

Revision	*Date*	*Description*
PA1	2025-11-03	First version.

2 Introduction

This document is a datasheet that specifies and describes the *iMX8M Mini DX-M1 SOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX8M Mini DX-M1 SOM Board* is a System-on-Module (SOM) based on NXP's ARM quad-core Cortex-A53 / M4 i.MX 8M Mini System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A53 / M4 based design. The Cortex-A53 cores run up to 1.8 GHz (1.6 GHz for industrial version) and the Cortex-M4 core at up to 400 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A53 cores and a Real-Time OS (RTOS) on the Cortex-M4. This architecture is ideal for real time applications where Linux cannot be used for all time critical tasks. The Cortex-M4 can handle (real time) critical tasks and can also be used to lower power consumption.

The *iMX8M Mini DX-M1 SOM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR4 memory sub-system reduces the power consumption.

The *iMX8M Mini DX-M1 SOM Board* has a small form factor and shields the user from a lot of complexity of designing a high-performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX8M Mini DX-M1 SOM Board* targets a wide range of applications, such as:

- Edge Compute applications
- Edge AI applications
- HMI/GUI solutions
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX8M Mini DX-M1 SOM Board*.

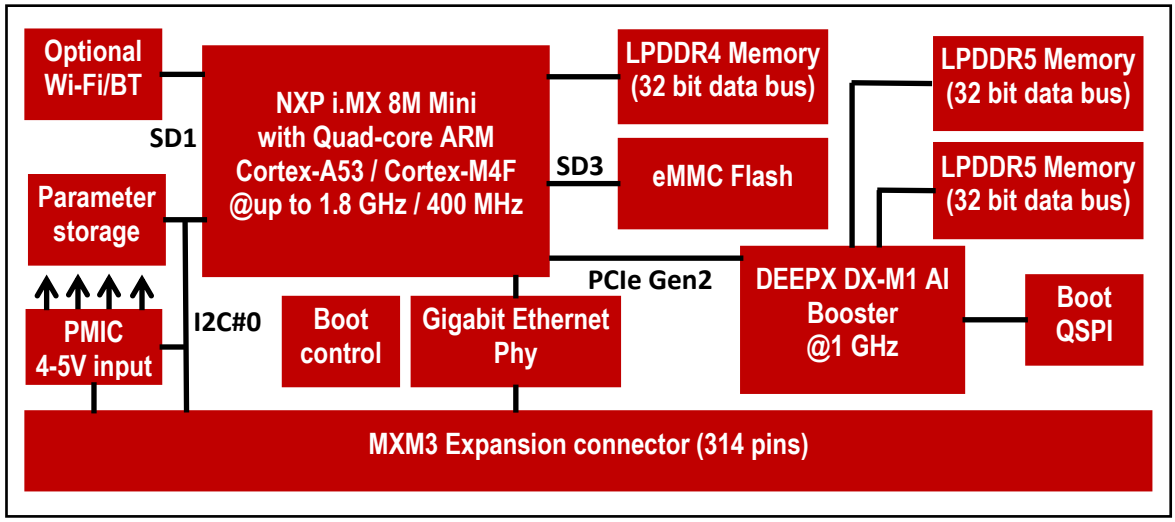


Figure 1 – iMX8M Mini DX-M1 SOM Board Block Diagram

The *iMX8M Mini DX-M1 SOM Board* pin assignment focuses on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four- or six-layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *SOM Boards* from Embedded Artists and the general, so called, EACOM specification is found in a separate document.

2.2 Software

The *iMX8M Mini DX-M1 SOM Board* has Board Support Packages (BSPs) for Embedded Linux and Android. Precompiled images are available. Embedded Artists work with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX8M Mini DX-M1 SOM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 8M Mini is a powerful SoC. The full specification can be found in NXP's *i.MX 8M Mini Datasheet* and *i.MX 8M Mini Reference Manual*. The table below lists the main features and functions of the *iMX8M Mini DX-M1 SOM board* - which represents Embedded Artists integration of the i.MX 8M Mini SoC. Due to pin configuration some functions and interfaces of the i.MX 8M Mini may not be available at the same time. See i.MX 8M Mini SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature		iMX8M Mini DX-M1 SOM Board
CPUs	NXP SoC	commercial temp. range industrial temp. range	MIMX8MM6DVTLZA (0 - 70° C) MIMX8MM6CVTKZA (-40 - 85° C)
	CPU Cores		4x Cortex-A53 1x Cortex-M4F with MPU/FPU
	L1 Instruction cache		32 KByte for each Cortex-A53 16 KByte on Cortex-M4
	L1 Data cache		32 KByte for each Cortex-A53

		16 KByte on Cortex-M4
	L2 Cache on Cortex-A53 cores	512 KByte
	On-chip SRAM (TCM for Cortex-M4)	256 KByte
	NEON SIMD media accelerator on Cortex-A53	✓
	Maximum CPU frequency	1.8/1.6 GHz on Cortex-A53 cores 400 MHz on Cortex-M4
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage	✓
	System JTAG controller	✓
	Resource Domain Controller (RDC)	✓
Memory	LPDDR4 RAM Size	4 GByte, default. Other on request.
	LPDDR4 RAM Speed	3000 MT/s
	LPDDR4 RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	32 GByte, default. Other on request.
Graphical Processing	Multimedia Graphics Processing Unit (GPU)	GCNanoUltra/GC320, OpenGL ES2.0/1.1, OpenVG1.1
	Video Decode Acceleration	1080p60 H.265, H.264, VP8, VP9
	Video Encode Acceleration	1080p60 H.264, VP8
Graphical Output	MIPI-DSI, 4 lanes	✓ up to 1080p60 resolution
Graphical Input	MIPI-CSI, 4 lanes	✓
Communication	Ethernet	1000/100/10 Mbps Gigabit Ethernet controller with support for EEE, Audio Video Bridging (AVB) and IEEE1588. On-board Gigabit PHY based on Realtek RTL8211FDI
	Wi-Fi/BT - optional	Optional Murata LBEE5HY2FY (2FY), 802.11a/b/g/n/ac/ax SISO, Wi-Fi 6E and 5.4 BR/EDR/BLE, SDIO interface, based on Infineon chipset CYW55513
AI Booster	NPU - optional	DEEPX DX-M1 AI Booster, up to 25TOPS. Frequency up to 1 GHz
	SDRAM - optional	4GByte LPDDR5 5600MT/s, 64-bit/4ch databus

Connectivity Interfaces (all functions are not available at the same time)	2x USB2.0 OTG port with Phy	✓
	1x PCIe Gen2 (1 lane)	**Note:** Available of DX-M1 AI Booster not mounted. If the AI Booster is mounted, the PCIe interface is used to communicate with the DX-M1.
	QuadSPI with support for XIP	✓
	5x I2S/SAI, SPDIF, 8-ch PDM	✓
	2x SD3.0/MMC 5.0	✓ SD3 interface used on-board to eMMC, SD1 interface used when on-board Wi-Fi/BT mounted
	3x SPI, 4x UART, 4x I²C	✓
	PWMs, WDOG	✓
Other	PMIC (BD71847MWV) supporting DVFS techniques for low power modes	✓
	E2PROM storing board information and Ethernet MAC address	✓
	On-board RTC via PMIC (BD71847MWV)	✓
	On-board watchdog functionality	✓

2.4 Reference Documents

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX8MMCEC, i.MX 8M Mini Applications Processors - Consumer Products Data Sheet, latest revision
- IMX8MMIEC, i.MX 8M Mini Applications Processors - Industrial Products Data Sheet, latest revision
- IMX8MMRM, i.MX 8M Mini Applications Processors Reference Manual, latest revision
- IMX8MMSRM, Security Reference Manual for i.MX 8M Mini, latest revision
- IMX8MMCE, Chip Errata for the i.MX 8M Mini, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12410, i.MX 8M Mini Power Consumption Measurement, latest revision
- AN12468, i.MX 8M Mini Product Lifetime Usage, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)

- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has created the *EACOM Board Specification* that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the EACOM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the EACOM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

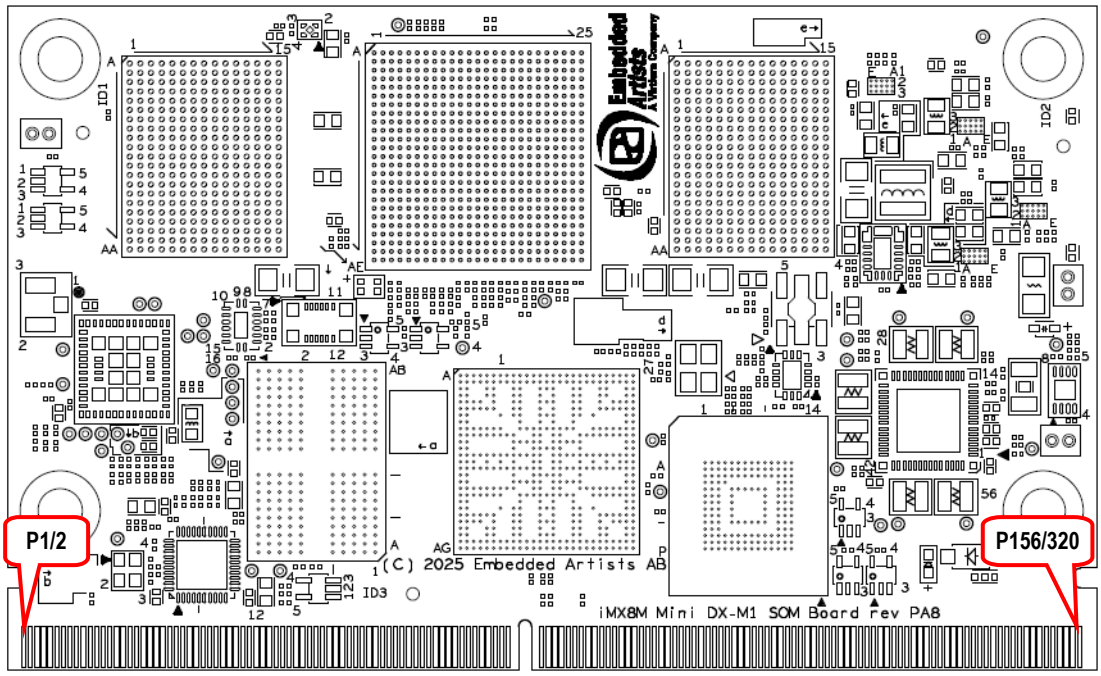


Figure 2 – EACOM Board Pin Numbering, Top Side

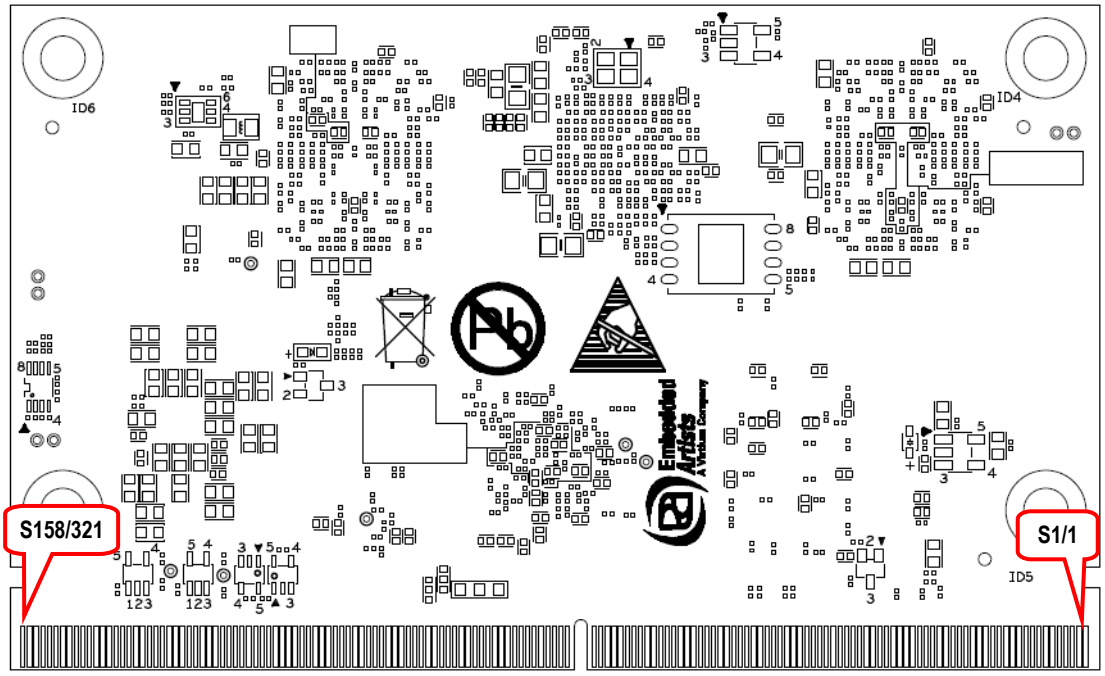


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different EACOM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 8M Mini Ball Name	The name of the i.MX 8M Mini SoC ball (or other component on the EACOM board) that is connected to this pin.
Alternative Pin Function	Information if the signal is a dedicated interface or a general pin that can multiples different signals. See a separate Excel sheet for details about available multiplexing alternatives.
Notes	When relevant, the preferred pin function is listed.

There are 54 ground pins, which is about 17%, and 10 input supply voltage pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	i.MX 8M Mini Ball Name	Alternative pin functions?	Notes
P1/2	GPIO-F	GPIO7	Yes	Controlled by alternative pin function GPIO1_IO7.
P2/4	GPIO-E	GPIO6	Yes	Controlled by alternative pin function GPIO1_IO6

P3/6	GPIO-D	SD2_NCD	Yes	Controlled by alternative pin function GPIO2_IO12. **Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra high-speed SD memory card.
P4/8	GPIO-C	SD2_NRST	Yes	Controlled by alternative pin function GPIO2_IO19. **Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra high-speed SD memory card. **Note:** This pin has a 4.7Kohm pull-up resistor to NVCC_SD2.
P5/10	SD_D1	SD2_D1	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P6/12	SD_D0	SD2_D0	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P7/14	SD_CLK	SD2_CLK	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P8/16	SD_CMD	SD2_CMD	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P9/18	SD_D3	SD2_D3	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P10/20	SD_D2	SD2_D2	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P11/22	SD_VCC	NVCC_SD2		Supply voltage for SD interface (1.85V or 3.2V). This is an output but should never be used to anything else than possible pullup resistors on the SD interface (SD2 in the i.MX8M Mini SoC).
P12/24	MMC_D1	SD1_D1	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P13/26	MMC_D0	SD1_D0	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P14/28	MMC_D7	SD1_D7	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P15/30	MMC_D6	SD1_D6	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P16/32	MMC_CLK	SD1_CLK	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P17/34	MMC_D5	SD1_D5	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P18/36	MMC_CMD	SD1_CMD	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P19/38	MMC_D4	SD1_D4	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P20/40	MMC_D3	SD1_D3	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P21/42	MMC_D2	SD1_D2	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted.

				Note: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P22/44	GND			
P23/46	HDMI_TXC_N			Not connected
P24/48	HDMI_TXC_P			Not connected
P25/50	GND			
P26/52	HDMI_TXD0_N			Not connected
P27/54	HDMI_TXD0_P			Not connected
P28/56	HDMI_HPD			Not connected
P29/58	HDMI_TXD1_N			Not connected
P30/60	HDMI_TXD1_P			Not connected
P31/62	GND			
P32/64	HDMI_TXD2_N			Not connected
P33/66	HDMI_TXD2_P			Not connected
P34/68	HDMI_CEC			Not connected
P35/70	GND			
P36/72	ETH1_MD1_P	ETH_TRXP1	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 4
P37/74	ETH1_MD1_N	ETH_TRXN1	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 5
P38/76	GND			
P39/78	ETH1_MD0_P	ETH_TRXP0	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 1
P40/80	ETH1_MD0_N	ETH_TRXN0	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 2
P41/82	ETH1_LINK1000	ETH_LED1000	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 33 **Note**: The signal has a 4.7Kohm pull-down resistor. It is not allowed to pull this signal high externally.
P42/84	ETH1_ACT	ETH_LEDACT	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 34 **Note**: The signal is a push-pull output. It is not allowed to pull this signal high or low externally.
P43/86	ETH1_LINK	ETH_LED10_100	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 32 **Note**: The signal has a 4.7Kohm pull-down resistor. It is not allowed to pull this signal high externally.
P44/88	ETH1_MD3_N	ETH_TRXN3	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 10
P45/90	ETH1_MD3_P	ETH_TRXP3	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 9
P46/92	GND			
P47/94	ETH1_MD2_N	ETH_TRXN2	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 7
P48/96	ETH1_MD2_P	ETH_TRXP2	No	Connects to Ethernet-PHY RTL8211FDI-CG, pin 6
P49/98	GND			
P50/100	ETH2_MD1_P			Not connected
P51/102	ETH2_MD1_N			Not connected
P52/104	GND			
P53/106	ETH2_MD0_P			Not connected
P54/108	ETH2_MD0_N			Not connected
P55/110	ETH2_LINK1000			Not connected
P56/112	ETH2_ACT			Not connected
P57/114	ETH2_LINK			Not connected

P58/116	ETH2_MD3_N			Not connected
P59/118	ETH2_MD3_P			Not connected
P60/120	GND			
P61/122	ETH2_MD2_N			Not connected
P62/124	ETH2_MD2_P			Not connected
P63/126	GND			
P64/128	USB_O1_DN	USB1_DN	No	
P65/130	USB_O1_DP	USB1_DP	No	
P66/132	USB_O1_OTG_ID	USB1_ID	No	
P67/134	USB_O1_SSTXN			Not connected
P68/136	USB_O1_SSTXP			Not connected
P69/138	GND			
P70/140	USB_O1_SSRXN			Not connected
P71/142	USB_O1_SSRXP			Not connected
P72/144	USB_O1_VBUS	USB1_VBUS	No	**Note**: This supply voltage must be connected to the USB1 interface to operate. The signal is 5V tolerant.
P73/146	USB_O1_PWR_EN	GPIO12	Yes	Controlled by alternative pin function GPIO1_IO12 (because Linux requires a GPIO for this function).
P74/148	USB_O1_OC	GPIO13	Yes	Controlled by alternative pin function USB1_OC
150	Non existing pin			
152	Non existing pin			
154	Non existing pin			
156	Non existing pin			
P75/158	USB_H1_PWR_EN	GPIO11	Yes	Controlled by alternative pin function GPIO1_IO11 (because Linux requires a GPIO for this function)
P76/160	USB_H1_OC	GPIO15	Yes	Controlled by alternative pin function USB2_OC
P77/162	GND			
P78/164	USB_H1_DN	USB2_DN	No	
P79/166	USB_H1_DP	USB2_DP	No	
P80/168	USB_H1_SSTXN			Not connected
P81/170	USB_H1_SSTXP	USB2_ID	No	**Note**: Non-standard pin allocation (USB_H1 is defined as a USB3 interface without ID-pin while the iMX8M Mini has a second USB2.0 OTG interface and needs an ID-pin).
P82/172	GND			
P83/174	USB_H1_SSRXN			Not connected
P84/176	USB_H1_SSRXP			Not connected
P85/178	USB_H1_VBUS	USB2_VBUS	No	**Note**: This supply voltage must be connected to the USB2 interface to operate. The signal is 5V tolerant.
P86/180	USB_H2_PWR_EN			Not connected
P87/182	USB_H2_OC			Not connected
P88/184	GND			
P89/186	USB_H2_DN			Not connected
P90/188	USB_H2_DP			Not connected
P91/190	GND			
P92/192	COM board specific	NVCC_RF		External power supply input to (optional) Wi-Fi/BT module. Not

				connected if no Wi-Fi/BT module is mounted.
P93/194	COM board specific	NVCC_RF		External power supply input to (optional) Wi-Fi/BT module. Not connected if no Wi-Fi/BT module is mounted.
P94/196	COM board specific	GND		
P95/198	COM board specific	GND		
P96/200	COM board specific	NVCC_1V8		1.8V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P97/202	COM board specific	NVCC_1V8		1.8V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P98/204	COM board specific	GND		
P99/206	COM board specific	GND		
P100/208	COM board specific	NVCC_3V3		3.3V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P101/210	COM board specific	NVCC_3V3		3.3V power supply generated on SOM, available for the carrier board. See chapter 7 and 8 for technical details.
P102/212	COM board specific	GND		
P103/214	COM board specific	GND		
P104/216	COM board specific	BT_PCM_OUT	No	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P105/218	COM board specific	BT_PCM_CLK	No	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P106/220	COM board specific	BT_PCM_IN	No	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P107/222	COM board specific	BT_PCM_SYNC	No	Connected to PCM interface of Wi-Fi/BT module, if mounted. **Note:** Signal is 1.8V logic
P108/224	COM board specific	M1_PWR_EN	No	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Connected to signal SD2_WP. **Note**: Logic level (3.3V or 1.8V depends on NVCC_SD1, which is controlled by the Linux BSP.
P109/226	COM board specific	M1_PCIE_RST	No	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Connected to signal NAND_DATA02. **Note:** Signal is 1.8V logic
P110/228	COM board specific	M1_PCIE_WAKE_N_OD	No	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Connected to signal NAND_DATA03. Signal is driven by the DX-M1. **Note:** Signal is 1.8V logic
P111/230	COM board specific	PCIE_CLKREQ_N_OD	No	This signal shall not be used if the DX-M1 AI accelerator is mounted. Even if the DX-M1 is not mounted, the signal should not be used to keep the design future-proof. Connected to signal I2C4_SCL. Signal is driven by the DX-M1. **Note:** Signal is 1.8V logic
P112/232	COM board specific	CLK_32K_OUT	No	32.768kHz clock signal from BD71847AMWV PMIC, pin 29. If using this signal externally on the carrier board use a buffer to minimize load in the signal.

				Note that the voltage level is 1.8V.
P113/234	COM board specific	I2C4_SDA	Yes	Controlled by alternative pin function GPIO5_IO21
P114/236	COM board specific			Do not connect to this signal.
P115/238	COM board specific	PWRON_B	No	Signal connects to the PWRON_B input on BD71847AMWV PMIC. **Note:** Signal is 1.8V logic and has a 100Kohm pull-up resistor to an internally generated 1.8V supply (SNVS_1V8).
P116/240	COM board specific			Do not connect to this signal.
P117/242	COM board specific			Do not connect to this signal.
P118/244	GND			
P119/246	SPI-B_SSEL	ECSPI2_SS0	Yes	Controlled by alternative pin function ECSPI2_SS0
P120/248	SPI-B_MOSI	ECSPI2_MOSI	Yes	Controlled by alternative pin function ECSPI2_MOSI
P121/250	SPI-B_MISO	ECSPI2_MISO	Yes	Controlled by alternative pin function ECSPI2_MISO
P122/252	SPI-B_CLK	ECSPI2_SCLK	Yes	Controlled by alternative pin function ECSPI2_SCLK
P123/254	SPI-A_SSEL	ECSPI1_SS0	Yes	Controlled by alternative pin function ECSPI1_SS0
P124/256	SPI-A_MOSI	ECSPI1_MOSI	Yes	Controlled by alternative pin function ECSPI1_MOSI
P125/258	SPI-A_MISO	ECSPI1_MISO	Yes	Controlled by alternative pin function ECSPI1_MISO
P126/260	SPI-A_CLK	ECSPI1_SCLK	Yes	Controlled by alternative pin function ECSPI1_SCLK
P127/262	GND			
P128/264	UART-C_RXD	UART4_RXD	Yes	Controlled by alternative pin function UART4_RXD **Note:** Signal is typically used for Cortex-M console.
P129/266	UART-C_TXD	UART4_TXD	Yes	Controlled by alternative pin function UART4_TXD **Note:** Signal is typically used for Cortex-M console.
P130/268	UART-B_RXD	UART1_RXD	Yes	Controlled by alternative pin function UART1_RXD **Note:** Signal is typically used for Bluetooth module UART interface.
P131/270	UART-B_CTS	UART4_RXD	Yes	Controlled by alternative pin function UART1_CTS_B **Note:** Signal is typically used for Bluetooth module UART interface.
P132/272	UART-B_RTS	UART4_TXD	Yes	Controlled by alternative pin function UART1_RTS_B **Note:** Signal is typically used for Bluetooth module UART interface.
P133/274	UART-B_TXD	UART2_TXD	Yes	Controlled by alternative pin function UART1_TXD **Note:** Signal is typically used for Bluetooth module UART interface.
P134/276	UART-A_RXD	UART2_TXD	Yes	Controlled by alternative pin function UART2_RXD **Note:** Signal is typically used for the Linux console (Cortex-A).
P135/278	UART-A_CTS	SAI3_RXC	Yes	Controlled by alternative pin function GPIO4_IO29
P136/280	UART-A_RTS	SAI3_RXD	Yes	Controlled by alternative pin function GPIO4_IO30
P137/282	UART.A_TXD	UART2_TXD	Yes	Controlled by alternative pin function UART2_TXD **Note:** Signal is typically used for the Linux console (Cortex-A).
P138/284	PWM	GPIO1	Yes	Controlled by alternative pin function PWM1_OUT
P139/286	GPIO-B	GPIO8	Yes	Controlled by alternative pin function GPIO1_IO8
P140/288	GPIO-A	GPIO0	Yes	Controlled by alternative pin function GPIO1_IO0
P141/290	PERI_PWR_EN			Enable signal (active high) for carrier board peripheral power supplies. This output is connected to an internally generated 3.3V supply.

		Note: When this supply is logically high (3.3V), external circuitry that drives any MXM3 pin can also be powered.
P142/292	RESET_IN	Reset input, active low. Pull signal low to activate reset. There is no need to pull signal high externally. There is a weak (400Kohm) pull-up resistor to VIN on this signal.
P143/294	RESET_OUT	Reset (open drain) output, active low. Driven low during reset. There is no pull-up resistor. An external pull-up resistor is needed with minimum value of 1 Kohm. The supply voltage to connect to can be anywhere between 1.8 to 5V.
P144/296	VIN_SELECT	This output is connected to VIN via a 1Kohm resistor to signal that supply voltage VIN shall be 4.2-5V. This signal can be used by carrier boards that can support EACOM boards that require 3.3V on VIN (in this case, this pin is connected to ground). If only the SOM board family shall be supported, which is the normal case, ignore this pin and do not connect to it.
P145/298	VBAT_RTC	Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	ISP_ENABLE	Should be left open (will write protect the on-board parameter storage E2PROM) or connected to GND (will enable writes to the on-board parameter storage E2PROM and place the i.MX 8M Mini SoC in USB OTG boot mode after a power cycle).
P147/302	VIN	Main input voltage supply (5V)
P148/304	VIN	Main input voltage supply (5V)
P149/306	VIN	Main input voltage supply (5V)
P150/308	VIN	Main input voltage supply (5V)
P151/310	VIN	Main input voltage supply (5V)
P152/312	VIN	Main input voltage supply (5V)
P153/314	VIN	Main input voltage supply (5V)
P154/316	VIN	Main input voltage supply (5V)
P155/318	VIN	Main input voltage supply (5V)
P156/320	VIN	Main input voltage supply (5V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	i.MX 8M Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	SAI2_RXFS	Yes	Controlled by alternative pin function GPIO4_IO21
S2/3	MQS_LEFT	SAI2_RXC	Yes	Controlled by alternative pin function GPIO4_IO22
S3/5	GND			
S4/7	AUDIO_TXFS	SAI2_TXFS	Yes	Controlled by alternative pin function SAI2_TXFS
S5/9	AUDIO_RXD	SAI2_RXD	Yes	Controlled by alternative pin function SAI2_RXD
S6/11	AUDIO_TXC	SAI2_TXC	Yes	Controlled by alternative pin function SAI2_TXC
S7/13	AUDIO_TXD	SAI2_TXD	Yes	Controlled by alternative pin function SAI2_TXD
S8/15	AUDIO_MCLK	SAI2_MCLK	Yes	Controlled by alternative pin function SAI2_MCLK
S9/17	GND			
S10/19	SPDIF_IN	SPDIF_RX	Yes	Controlled by alternative pin function SPDIF_RX
S11/21	SPDIF_OUT	SPDIF_TX	Yes	Controlled by alternative pin function SPDIF_TX
S12/23	CAN2_TX	SAI5_RXD3	Yes	Controlled by alternative pin function GPIO3_IO24

S13/25	CAN2_RX	SAI5_MCLK	Yes	Controlled by alternative pin function GPIO3_IO25
S14/27	CAN1_TX	SAI5_RXD1	Yes	Controlled by alternative pin function GPIO3_IO22
S15/29	CAN1_RX	SAI5_RXD2	Yes	Controlled by alternative pin function GPIO3_IO23
S16/31	GND			
S17/33	LVDS1_D3_P			
S18/35	LVDS1_D3_N			
S19/37	GPIO-J	SD1_STROBE_EXT	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function GPIO2_IO11
S20/39	LVDS1_D2_P			
S21/41	LVDS1_D2_N			
S22/43	GND			
S23/45	LVDS1_D1_P			
S24/47	LVDS1_D1_N			
S25/49	GND			
S26/51	LVDS1_D0_P			
S27/53	LVDS1_D0_N			
S28/55	GND			
S29/57	LVDS1_CLK_P			
S30/59	LVDS1_CLK_N			
S31/61	GND			
S32/63	LVDS0_D3_P			
S33/65	LVDS0_D3_N			
S34/67	GPIO-H	SD1_NRST_EXT	Yes	Pin is only available if no on-board Wi-Fi/BT module is mounted. Controlled by alternative pin function GPIO2_IO10
S35/69	LVDS0_D2_P			
S36/71	LVDS0_D2_N			
S37/73	GND			
S38/75	LVDS0_D1_P			
S39/77	LVDS0_D1_N			
S40/79	GND			
S41/81	LVDS0_D0_P			
S42/83	LVDS0_D0_N			
S43/85	GND			
S44/87	LVDS0_CLK_P			
S45/89	LVDS0_CLK_N			
S46/91	I2C-A_SDA	I2C1_SDA	No	Controlled by alternative pin function I2C1_SDA. Signal must be I2C1_SDA since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S47/93	I2C-A_SCL	I2C1_SCL	No	Controlled by alternative pin function I2C1_SCL. Signal must be I2C1_SCL since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S48/95	I2C-B_SDA	I2C2_SDA	Yes	Controlled by alternative pin function I2C2_SDA

				Note: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S49/97	I2C-B_SCL	I2C2_SCL	Yes	Controlled by alternative pin function I2C2_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S50/99	HDMI/I2C-C_SDA	I2C3_SDA	Yes	Controlled by alternative pin function I2C3_SDA **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S51/101	HDMI/I2C-C_SCL	I2C3_SCL	Yes	Controlled by alternative pin function I2C3_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S52/103	TP_RST	GPIO5	Yes	Controlled by alternative pin function GPIO1_IO5
S53/105	TP_IRQ	SPDIF_EXT_CLK	Yes	Controlled by alternative pin function GPIO5_IO5
S54/107	DISP_PWR_EN	SAI5_RXD0	Yes	Controlled by alternative pin function GPIO3_IO21
S55/109	BL_PWR_EN	GPIO9	Yes	Controlled by alternative pin function GPIO1_IO9
S56/111	BL_PWM	GPIO14-PWM3_OUT	Yes	Controlled by alternative pin function PWM3_OUT
S57/113	GND			
S58/115	LCD_R0	SAI5_RXFS	Yes	Controlled by alternative pin function GPIO3_IO19
S59/117	LCD_R1	SAI5_RXC	Yes	Controlled by alternative pin function GPIO3_IO20
S60/119	LCD_R2	SAI3_RXFS	Yes	Controlled by alternative pin function GPIO4_IO28
S61/121	LCD_R3	SAI3_TXD	Yes	Controlled by alternative pin function GPIO5_IO1
S62/123	LCD_R4	SAI3_TXC	Yes	Controlled by alternative pin function GPIO5_IO0
S63/125	LCD_R5	SAI3_TXFS	Yes	Controlled by alternative pin function GPIO4_IO31
S64/127	LCD_R6	SAI3_MCLK	Yes	Controlled by alternative pin function GPIO5_IO2
S65/129	LCD_R7	SAI1_RXD7	Yes	Controlled by alternative pin function GPIO4_IO9
S66/131	LCD_G0	SAI1_RXD6	Yes	Controlled by alternative pin function GPIO4_IO8
S67/133	LCD_G1	SAI1_RXD5	Yes	Controlled by alternative pin function GPIO4_IO7
S68/135	LCD_G2	SAI1_RXD4	Yes	Controlled by alternative pin function GPIO4_IO6
S69/137	LCD_G3	SAI1_RXD3	Yes	Controlled by alternative pin function GPIO4_IO5
S70/139	LCD_G4	SAI1_RXD2	Yes	Controlled by alternative pin function GPIO4_IO4
S71/141	LCD_G5	SAI1_RXD1	Yes	Controlled by alternative pin function GPIO4_IO3
S72/143	LCD_G6	SAI1_RXD0	Yes	Controlled by alternative pin function GPIO4_IO2
S73/145	LCD_G7	SAI1_RXC	Yes	Controlled by alternative pin function GPIO4_IO1
S74/147	GND			
S75/149	LCD_B0	SAI1_RXFS	Yes	Controlled by alternative pin function GPIO4_IO0
151	Non existing pin			
153	Non existing pin			
155	Non existing pin			
S76/157	LCD_B1	SAI1_TXD7	Yes	Controlled by alternative pin function GPIO4_IO19
S77/159	LCD_B2	SAI1_TXD6	Yes	Controlled by alternative pin function GPIO4_IO18
S78/161	LCD_B3	SAI1_TXD5	Yes	Controlled by alternative pin function GPIO4_IO17
S79/163	LCD_B4	SAI1_TXD4	Yes	Controlled by alternative pin function GPIO4_IO16
S80/165	LCD_B5	SAI1_TXD3	Yes	Controlled by alternative pin function GPIO4_IO15
S81/167	LCD_B6	SAI1_TXD2	Yes	Controlled by alternative pin function GPIO4_IO14

S82/169	LCD_B7	SAI1_TXD1	Yes	Controlled by alternative pin function GPIO4_IO13
S83/171	LCD_CLK	SAI1_MCLK	Yes	Controlled by alternative pin function GPIO4_IO20
S84/173	GPIO-G			
S85/175	LCD_HSYNC	SAI1_TXFS	Yes	Controlled by alternative pin function GPIO4_IO10
S86/177	LCD_VSYNC	SAI1_TXC	Yes	Controlled by alternative pin function GPIO4_IO11
S87/179	LCD_ENABLE	SAI1_TXD0	Yes	Controlled by alternative pin function GPIO4_IO12
S88/181	GND			
S89/183	AIN_VREF			Not connected
S90/185	AIN7			Not connected
S91/187	AIN6			Not connected
S92/189	AIN5			Not connected
S93/191	AIN4			Not connected
S94/193	AIN3			Not connected
S95/195	AIN2			Not connected
S96/197	AIN1			Not connected
S97/199	AIN0			Not connected
S98/201	GND			
S99/203	COM board specific	MIPI_DSI_D0N	No	
S100/205	COM board specific	MIPI_DSI_D0P	No	
S101/207	GND			
S102/209	COM board specific	MIPI_DSI_D1N	No	
S103/211	COM board specific	MIPI_DSI_D1P	No	
S104/213	GND			
S105/215	COM board specific	MIPI_DSI_CLKN	No	
S106/217	COM board specific	MIPI_DSI_CLKP	No	
S107/219	COM board specific	GND		
S108/221	COM board specific	MIPI_DSI_D2N	No	
S109/223	COM board specific	MIPI_DSI_D2P	No	
S110/225	COM board specific	GND		
S111/227	COM board specific	MIPI_DSI_D1N	No	
S112/229	COM board specific	MIPI_DSI_D1P	No	
S113/231	COM board specific	GND		
S114/233	CSI_HSYNC	POR_B	No	Signal connects to the POR_B input on the i.MX8M Mini SoC and the BD71847AMWV PMIC. **Note:** Signal is 1.8V logic and has a 100Kohm pull-up resistor to an internally generated 1.8V supply (SNVS_1V8). This signal should only be driven low. On most integrations, this pin shall not be connected. Non-standard pin allocation.
S115/235	CSI_VSYNC	JTAG_TRST	No	Signal connects to the JTAG_TRST pin on the i.MX8M Mini SoC. **Note:** Signal is 1.8V logic. Non-standard pin allocation.
S116/237	CSI_MCLK	JTAG_TDO	No	Signal connects to the JTAG_TDO pin on the i.MX8M Mini SoC.

				Note: Signal is 1.8V logic. Non-standard pin allocation.
S117/239	CSI_PCLK	JTAG_TDI	No	Signal connects to the JTAG_TDI pin on the i.MX8M Mini SoC. **Note:** Signal is 1.8V logic. Non-standard pin allocation.
S118/241	GND			
S119/243	CSI_D0	JTAG_TMS	No	Signal connects to the JTAG_TMS pin on the i.MX8M Mini SoC. **Note:** Signal is 1.8V logic. Non-standard pin allocation.
S120/245	CSI_D1	JTAG_TCK	No	Signal connects to the JTAG_TCK pin on the i.MX8M Mini SoC. **Note:** Signal is 1.8V logic. Non-standard pin allocation.
S121/247	CSI_D2	NVCC_JTAG	No	Connected to the internally generated 1.8V power supply. This is the signaling voltage of the JTAG interface. Non-standard pin allocation.
S122/249	CSI_D3			Do not connect to this pin.
S123/251	CSI_D4			Do not connect to this pin.
S124/253	CSI_D5			Do not connect to this pin.
S125/255	CSI_D6	NVCC_SNVS_1V8	No	Do not connect to this pin. Non-standard pin allocation.
S126/257	CSI_D7	ONOFF	No	Signal connects to the ONOFF input on the i.MX8M Mini SoC. **Note:** Signal is 1.8V logic and has a 100Kohm pull-up resistor to an internally generated 1.8V supply (SNVS_1V8). This signal should only be driven low. Non-standard pin allocation.
S127/259	GND			
S128/261	CSI_D3_M	MIPI_CSI1_D3N	No	
S129/263	CSI_D3_P	MIPI_CSI1_D3P	No	
S130/265	GND			
S131/267	CSI_D2_M	MIPI_CSI1_D2N	No	
S132/269	CSI_D2_P	MIPI_CSI1_D2P	No	
S133/271	GND			
S134/273	CSI_D1_M	MIPI_CSI1_D1N	No	
S135/275	CSI_D1_P	MIPI_CSI1_D1P	No	
S136/277	GND			
S137/279	CSI_D0_M	MIPI_CSI1_D0N	No	
S138/281	CSI_D0_P	MIPI_CSI1_D0P	No	
S139/283	GND			
S140/285	CSI_CLK_M	MIPI_CSI1_CLKN	No	
S141/287	CSI_CLK_P	MIPI_CSI1_CLKP	No	
S142/289	GND			
S143/291	SATA_TX_P			Not connected
S144/293	SATA_TX_N			Not connected
S145/295	GND			

S146/297	SATA_RX_N			Not connected
S147/299	SATA_RX_P			Not connected
S148/301	BOOT_CTRL		No	
S149/303	GND			
S150/305	PCIE_CLK_P	PCIE_CLK_P	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: 100MHz PCIe reference clock output. The signals require a 50 ohm termination resistor to ground at the receiver end.
S151/307	PCIE_CLK_N	PCIE_CLK_N	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: 100MHz PCIe reference clock output. The signals require a 50 ohm termination resistor to ground at the receiver end.
S152/309	GND			
S153/311	PCIE_TX_P	PCIE_TX_P	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S154/313	PCIE_TX_N	PCIE_TX_N	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe transmit output
S155/315	GND			
S156/317	PCIE_RX_P	PCIE_RX_P	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input
S157/319	PCIE_RX_N	PCIE_RX_N	No	If DX-M1 AI accelerator mounted: not connected If DX-M1 AI accelerator not mounted: PCIe receive input
S158/321	GND			

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 8M Mini SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leaves great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like MIPI-DSI, MIPI-CSI and USB. i.MX 8M Mini pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards, the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX8M Mini DX-M1 SOM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M Mini pin. For more information about the register settings, see the *i.MX 8M Mini Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *i.MX 8M Mini Application Processor Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the EACOM function allocation. The reset state is typically GPIO, ALT5 function, except for the GPIO1_IO01-15 signals that are ALT0 functions, but that is the GPIO function.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M Mini pin. For more information about the register settings, see the *i.MX 8M Mini Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, some with pull-down resistor, some without, and some with pull-up resistor, after reset. Some pins are configured as Hi-Z outputs. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

Also note that due to silicon revision errata in the i.MX8M Mini SoC, the pull-up and pull-down resistors are currently not functional when voltage level is 3.3V, which most of the signals are.

5 Interface Description

The **i.MX 8M Mini datasheet and reference manuals from NXP shall always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously. There is an accompanying Excel document that lists all alternative functions for each available I/O pin. It is recommended to study this document to get an overview of the available pin multiplexing options.

The process of defining the pin/function for a system is:

1. Define which interfaces are needed in the system.
2. Allocate each needed interface to either Cortex-A53 ("Linux side") or M4 side ("real-time side").
3. Consult the Excel sheet and allocate the interfaces to different pins.
    a. If possible, follow the EACOM pin and interface allocation. It is not strictly needed but will simplify if the SOM board will be replaced in a future update/upgrade.
    b. Note that connector JC (and signals allocated to this connector) will not exist if on-board Wi-Fi/BT module is mounted.
    c. Note that not all signals have 3.3V logic level. Some also have 1.8V logic level.
4. When a suitable pin/function allocation has been done, update the *.dts file under Linux to enable the interfaces that shall be controlled from the A53/Linux side. On the M4 side, peripherals are enabled and initialized via function calls, see the SDK for details.
    a. If pin/function allocation is impossible, the basic architecture under 1) must be reexamined and updated.

6 Boot Control

This chapter presents the different boot settings that the *iMX8M Mini DX-M1 SOM Board* supports.

Note that this chapter only presents how the different options are controlled. If does not discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *iMX8M Mini DX-M1 SOM Board* supports booting (i.e., from where the i.MX 8M Mini SoC starts downloading code to start executing from) from different sources:

1. On-board eMMC Flash, **which is the default**
2. USB OTG download (also called 'serial download')
3. Other sources, like external SD/MMC memory cards, etc.
   Note that the OTP fuses must be programmed to set the specific source.

Two signals control the booting source/process, BOOT_CTRL and ISP_ENABLE, see table below:

Boot source	BOOT_CTRL	ISP_ENABLE
Boot according to OTP fuses (eFuses) – default is to boot from the on-board eMMC • *iMX8M Mini uCOM Boards* are delivered with the OTP fuse: BT_FUSE_SEL be set to 1. The rest of the OTP fuses are left unprogrammed. • Just programming BT_FUSE_SEL to 1 will default to eMMC boot mode. Any boot mode supported by the i.MX 8M Mini SoC and the hardware connected to it can be selected. See *i.MX8M Mini Applications Processor Reference Manual* for details about available sources and OTP fuse settings. • Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery.	Do not care	Floating Jumper open on carrier board
USB OTG This is known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation. This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.	Do not care	LOW (grounded) Jumper inserted / shorted on carrier board

On a custom carrier board, it is recommended to connect signal BOOT_CTRL to the ground via a zero-ohm resistor. Never directly connected to ground. This would also make it easy to leave the pin floating, if needed.

6.1 SOM Carrier Board Boot Control Jumpers

The picture below describes where to find the two boot control jumpers on the SOM Carrier Board.

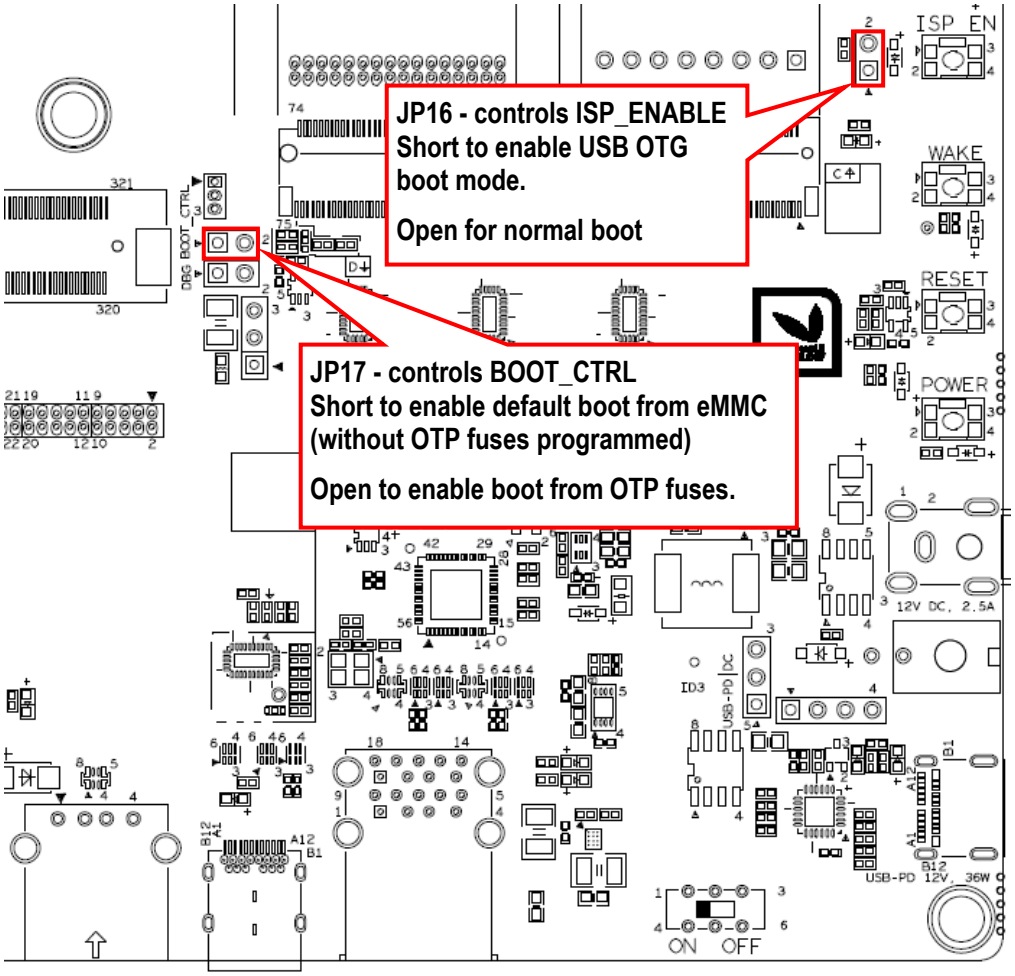


Figure 4 – SOM Carrier Board rev A, Boot Control Jumpers

7 Powering and PMIC Integration

The i.MX 8M Mini SoC is tightly integrated with the PMIC (BD71847MWV) to achieve high-performance and low-power operation of the *iMX8M Mini DX-M1 SOM Board*. The BD71847MWV PMIC is specifically developed for the i.MX 8M Mini SoC. It also includes a real-time clock. See the BD71847MWV datasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are available for the carrier board design, reducing integration costs. Designs with moderate power consumption may not need any external power supply at all. Everything can be handled by the on-board PMIC. Section 7.1 presents the available power rails.

7.1 Available Power Supply Rails

The table below presents the available power rails that can be used on the carrier board that the *iMX8M Mini DX-M1 SOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
NVCC_3V3 **on MXM3 pins P100/208 and P101/210**	3.3V for external use.	3.3V	750mA
NVCC_1V8 **on MXM3 pins P96/200 and P97/202**	1.8V for external use.	1.8V	500mA

For any of above supply next, connect to both MXM3 pins, respectively, on the expansion connector that carry a specific power rail.

Note that external load variations can affect the PMIC operation and potentially disturb the i.MX 8M Mini SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails. Also **calculate the heat dissipation** of the PMIC in case the carrier board has high current consumption.

8 Technical Specification

8.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	5.5	V
VBAT	RTC supply voltage	-0.3	5.5	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO	0	3.6	V
	Vin/Vout (I/O VDD + 0.3): 1.8V IO	0	1.98	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

8.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage	3.5	5.0	5.2	V
	Ripple with frequency content < 10 MHz			50	mV
	Ripple with frequency content ≥ 10 MHz			10	mV
VBAT	RTC supply voltage	3.5		5.0	V
	Note: This voltage must always remain valid for correct operation of the board (including but not limited to the RTC).				
USB_xx_VBUS	USB VBUS signals		5	5.25	V

8.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range of 1-20 ms.

8.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see *i.MX 8M Mini Datasheet*. The internal VDD operating point for GPIOs is 3.3V or 1.8V for all signals.

8.4.1 Reset Output Voltage Range

The reset output is an open drain output with no pull-up resistor. An external pull-up resistor is needed with minimum value of 1 Kohm. The supply voltage to connect to can be anywhere between 1.8 to 5V. Maximum output voltage when active is 0.4V.

8.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 10 uS minimum. The internal reset pulse will be 140-560 mS long, before the i.MX 8M Mini boot process starts.

8.5 Power Consumption

There are several factors that determine power consumption of the *iMX8M Mini DX-M1 SOM Board*, like input voltage, operating temperature, LPDDR4 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

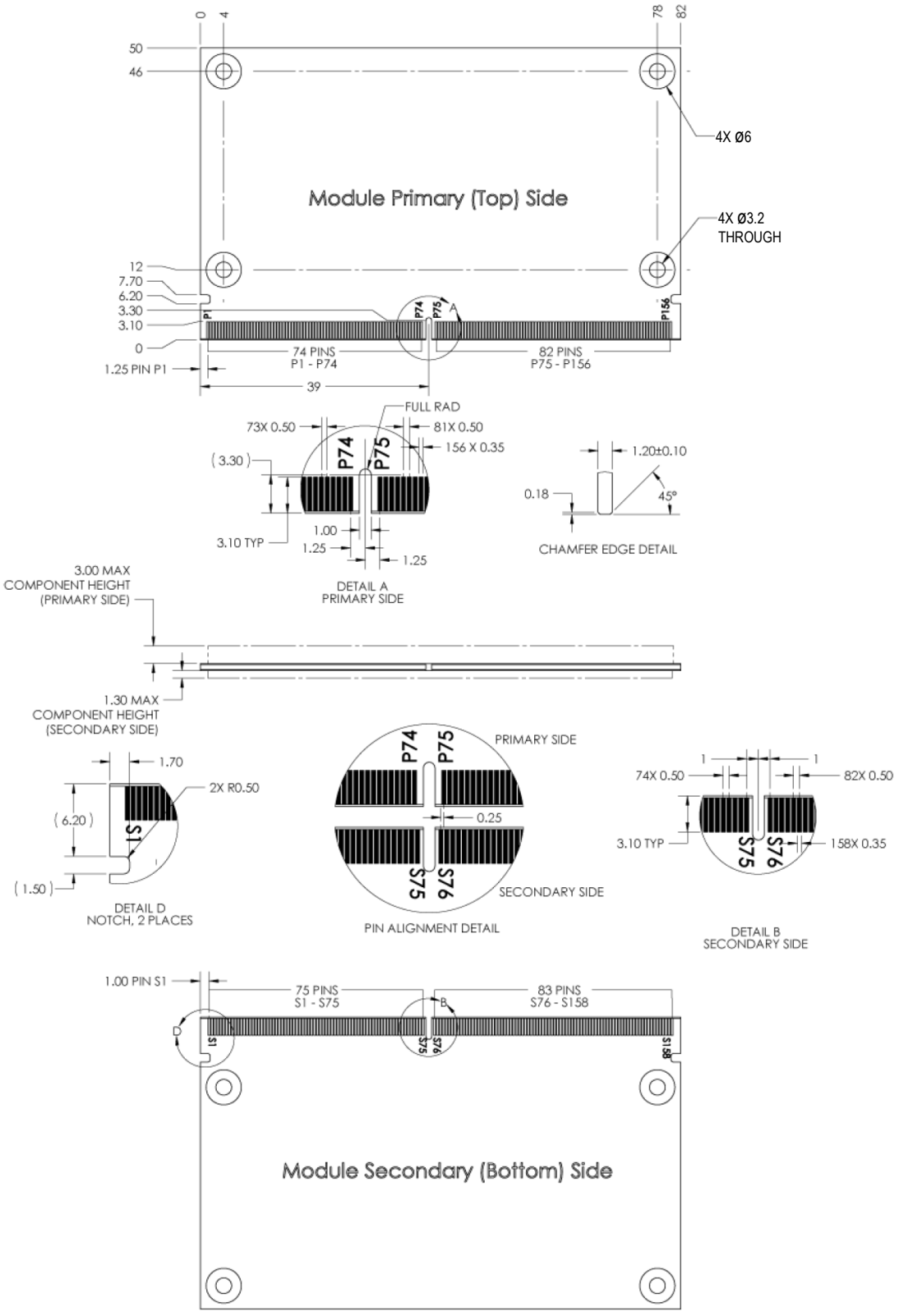
Symbol	Description (VIN = 4.2V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 1.8 GHz ARM frequency, without Ethernet		TBD	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		TBD TBD TBD	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA

8.6 Mechanical Dimensions

The board uses the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm
Module weight	16 ±1 gram	gram

The picture below illustrates the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and illustrates pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 5 – iMX8M Mini DX-M1 SOM Board Mechanical Outline

8.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers, at different board-to-board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE should not be used since this specific connector lacks some of the pins. It is, however, possible to use the connector if it is acceptable for the project not to use the following pins:

- P146/300 ISP_ENABLE This pin is also used to select USB OTG as boot mode (when pulled low), also known as "factory recovery" mode. Not having access to this pin means that USB OTG mode cannot be enabled from the carrier board.
- P147/302 VIN This is not a problem since there are many VIN pins.
- S149/303 GND This is not a problem since there are many GND pins.
- S148/301 GND This is not a problem since there are many GND pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the SOM Carrier board. This connector gives a board-to-board stacking height of 5.0 mm. This space allows some components to also be placed right under the SOM board.

Always check available component height before placing components on the carrier board under the SOM board, see picture below.

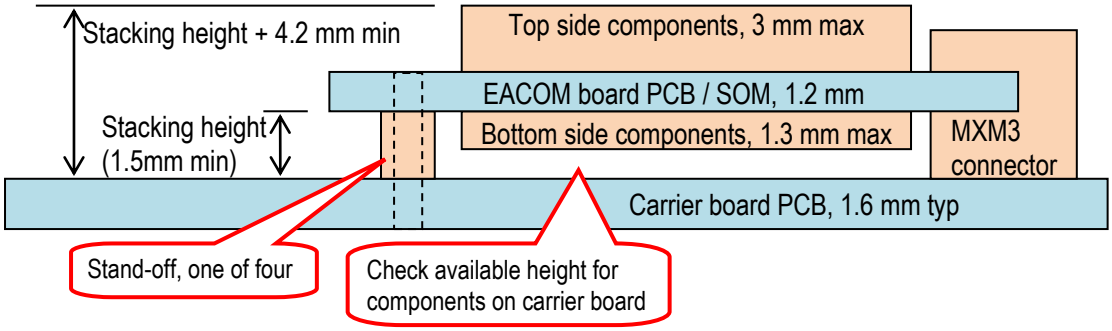


Figure 6 – SOM Board Mounting in MXM3 Connector, Stacking Height

8.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

Do not apply too high torque on the screws. That will create mechanical stress on the PCB and result on cracked BGA balls and/or cracked copper tracks. The order the screws are mounted and tightened is also very important. Do not tighten the screws immediately. Read the information in section 10.1 for details, including watching the YouTube video referred to.

8.7 Environmental Specification

8.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature i.MX 8M SoC, operating:	comm. temp. range ind. temp. range.	0 -40	95 105	°C °C

[1] Depends on cooling/heat management solution.

8.7.2 Relative Humidity (RH)

Parameter		Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 70°C, non-condensing Operating: -40°C ≤ T_A ≤ 85°C, non-condensing	(comm. temp. range) (ind. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing		5	90	%

8.8 Thermal Design Considerations

Heat dissipation from the i.MX 8M Mini SoC depends on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat can be up to 3 Watt but is typically much lower.

Whether external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *iMX8M Mini uCOM Board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 8M Mini SoC.

The i.MX 8M Mini SoC implements DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling via the Linux BSP. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general, this results in higher performance at lower average power consumption.

The i.MX 8M Mini SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affects several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: i.MX 8M Mini Dual Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

External cooling will most likely be needed – more information about this will be added in a future revision of the document, including information about the DX-M1 thermal management.

Be very careful when mounting the heat sink. Do not apply force so that the PCB will bend. That will result in immediate failure of boards or long-term reliability problems.

8.8.1 Thermal Parameters

The i.MX 8M Mini SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	22.9	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	4	°C/W

8.9 Product Compliance

Visit Embedded Artists' website at https://www.embeddedartists.com/product_compliance for up-to-date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

9 Functional Verification and RMA

There is a separate document that presents several functional tests that can be performed on the *iMX8M Mini DX-M1 SOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX8M Mini DX-M1 AI Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

10 Things to Note

This chapter presents a few issues and considerations that users must note.

10.1 Handle the SOM Board with Great Care

Handle the *iMX8M Mini DX-M1 SOM board* with great mechanical care. Only remove/unmount it from the *SOM Carrier board* if absolutely needed. Watch the YouTube video we have published about this topic: https://www.youtube.com/watch?v=6mvVnA3Chbw, title "How to mount and unmount a COM board". Note that in this context, we use the term SOM and COM interchangeable. Even though the video refers to COM boards, the exact same handling principles apply to our SOM boards.

10.2 Shared Pins and Multiplexing

The i.MX 8M Mini SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX8M Mini DX-M1 SOM* on-board design. Check if the interfaces needed are available to allocation before starting a design. See chapter 4 for details.

10.3 Only Use EA Board Support Package (BSP)

The *iMX8M Mini DX-M1 SOM board* uses multiple on-board interfaces in the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX8M Mini DX-M1 SOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

10.4 Boot Partition Size in eMMC

The size of the boot partition varies between different eMMC parts. The boot partition on parts mounted on the *iMX8M Mini DX-M1 SOM* will be 4MByte minimum. It can be larger but never assume it is larger than 4 Mbyte. Design your system to only require 4MByte to operate correctly.

10.5 OTP Fuse Programming

The i.MX 8M Mini SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 8M Mini Datasheet* and *iMX 8M Mini Reference Manual* for details. Once programmed, there is no possibility of reprograming them.

iMX8M Mini DX-M1 SOM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and, in that case, which ones.

Note that Embedded Artists does not replace iMX8M Mini DX-M1 SOM Boards because of wrong OTP programming. It's the user's responsibility to be certain before OTP programming and not to program the fuses by accident.

10.6 Write Protect on Parameter Storage E2PROM

There is an on-board I2C-E2PROM connected to I2C-channel #1 with 7-bit address 0x55 (8-bit address 0xAA/0xAB). The parameter storage E2PROM contains important system data like DDR

memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write-protected if signal ISP_ENABLE (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the i.MX 8M Mini SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

Note that it is not possible to connect an external I2C-device to IC2-channel #1 on the carrier board with this address (since this address is taken by the on-board parameter storage memory).

10.7 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX8M Mini DX-M1 SOM Board* targets a wide range of applications, such as:

- Edge Compute applications
- Edge AI applications
- HMI/GUI solutions
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX8M Mini DX-M1 SOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If you have an application in this area, contact Embedded Artists for a discussion.

If not before, **it is essential to contact Embedded Artists before production begins**. To ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX8M Mini DX-M1 SOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX8M Mini DX-M1 SOM Board*.

10.8 ESD Precaution when handling iMX8M Mini DX-M1 SOM Board

Please note that the *iMX8M Mini DX-M1 SOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel should handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the board to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

10.9 EMC / ESD

The *iMX8M Mini DX-M1 SOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless, depending on the target system, additional anti-interference measures may still be necessary to adhere to the limits for the overall system.

The *iMX8M Mini DX-M1 SOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only make sense on the complete solution.

No specific ESD protection has been implemented on the *iMX8M Mini DX-M1 SOM Board*. ESD protection on board level is the same as what is specified in the i.MX 8M Mini SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs and outputs of the system.

11 Custom Design

This document specifies the standard *iMX8M Mini DX-M1 SOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Mounting a Wi-Fi/BT module.
- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different board form factors, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are taller (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *iMX8M Mini DX-M1 SOM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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