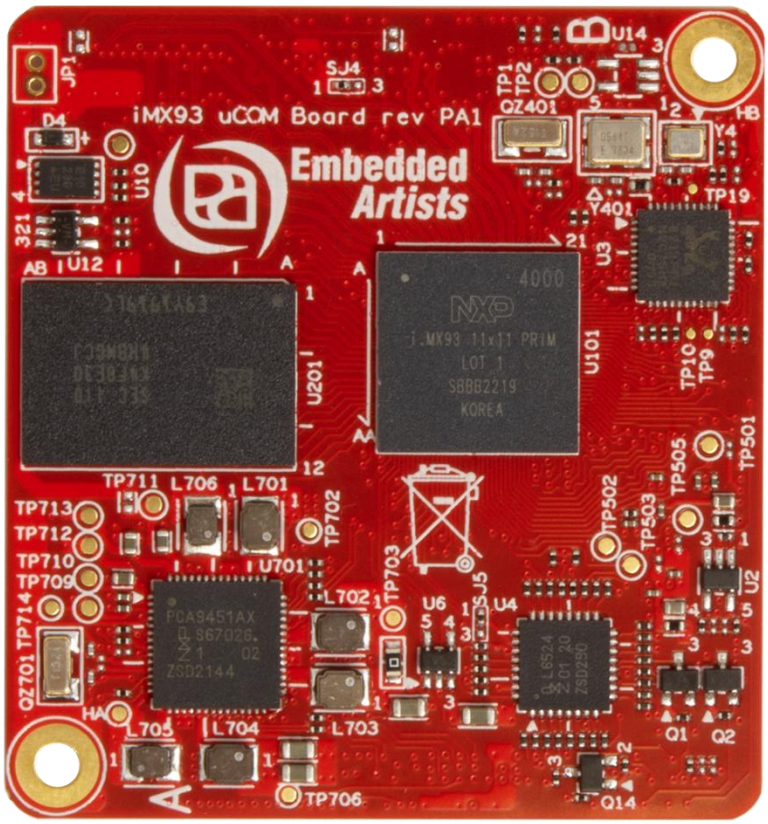
iMX93 uCOM Board Datasheet



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1 Document Revision History

Revision	*Date*	*Description*
PA1	2023-05-18	First version.
PA2	2023-05-22	Updated pin table.

2 Introduction

This document is a datasheet that specifies and describes the *iMX93 uCOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there is separate software development documentation that should also be consulted.

2.1 Hardware

The *iMX93 uCOM Board* is a Computer-on-Module (COM) based on NXP's ARM dual-core Cortex-A55 / M33 i.MX 93 System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A55 / M33 based design. The Cortex-A55 cores run at up to 1.7 GHz (1.5 GHz for industrial version) and the Cortex-M33 core at up to 250 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A55 cores and a Real-Time OS (RTOS) on the Cortex-M33. This architecture is ideal for real time applications where Linux cannot be used for all time critical tasks. The Cortex-M33 can handle (real time) critical tasks and can also be used to lower power consumption.

The *iMX93 uCOM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR4 memory sub-system reduce the power consumption.

The SoC is part of the scalable i.MX 93 product family. There is a range of i.MX RT/6/7/8/9 (u)COM Boards from Embedded Artists with single, dual and quad Cortex-A cores, with or without a heterogeneous Cortex-M core. Groups of boards (uCOM and COM) share the same basic pinning for maximum flexibility and performance scalability.

The *iMX93 uCOM Board* has an ultra-small form factor and shields the user from a lot of complexity of designing a high-performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX93 uCOM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Building Safety / Security
- Home appliances
- Robotic appliance
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll / Ticketing Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX93 uCOM Board*.

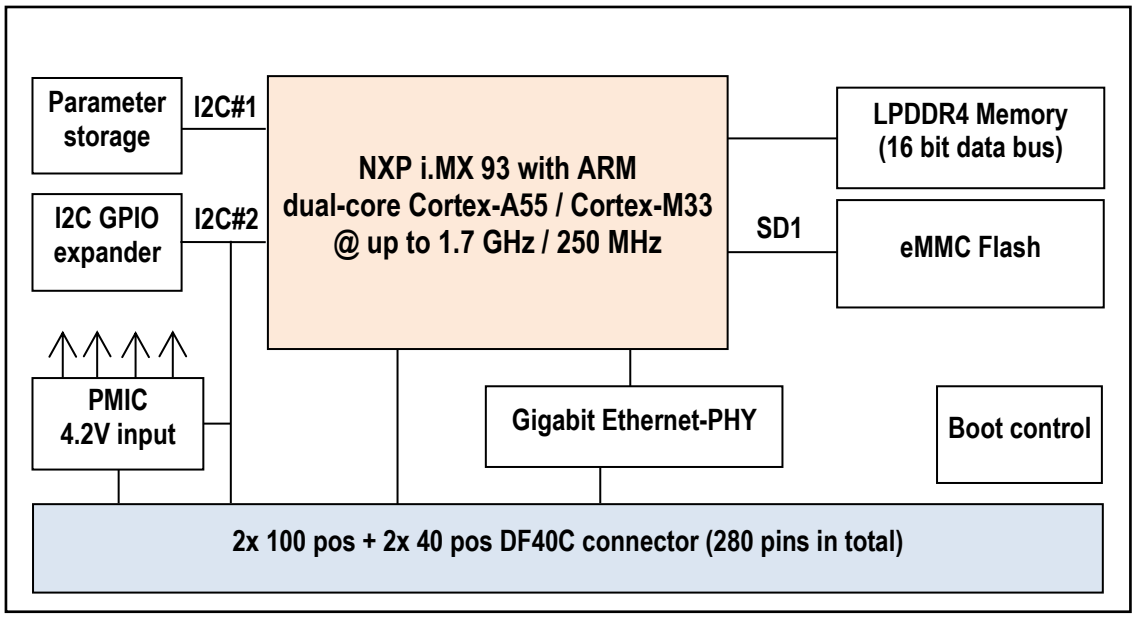

Figure 1 – iMX8M Mini uCOM Board Block Diagram

The *iMX93 uCOM Board* pin assignment focuses on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four-layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX RT/7/8/9 uCOM Boards* from Embedded Artists and the general, so called, EAuCOM specification is found in separate document.

2.2 Software

The *iMX93 uCOM Board* has Board Support Packages (BSPs) for Linux and and SDK for the Cortex-M33 side. Precompiled images are available. Embedded Artists work with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX93 uCOM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 93 is a powerful SoC. The full specification can be found in NXP's *i.MX 93 Datasheet* and *i.MX 93 Reference Manual*. The table below lists the main features and functions of the *iMX93 uCOM board* - which represents Embedded Artists integration of the i.MX 93 SoC. Due to pin configuration some functions and interfaces of the i.MX 93 may not be available at the same time. See i.MX 93 SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature		iMX93 uCOM Board
CPUs	NXP SoC	extended temp. range	MIMX9352CVUXMAA (-25 - 85° C)
	CPU Cores		2x Cortex-A55 1x Cortex-M33
	L1 Instruction cache		32 KByte for Cortex-A55 16 KByte for Cortex-M33

	L1 Data cache	32 KByte for Cortex-A55 16 KByte on Cortex-M33
	L2 Cache for Cortex-A55 cores	64 Kbyte per Cortex-A55 core
	L3 Cache for Cortex-A55 cores	256 Kbyte
	On-chip SRAM (TCM for Cortex-M33)	256 KByte
	NEON SIMD media accelerator on Cortex-A55	✓
	Maximum CPU frequency	1.7/1.5 GHz on Cortex-A55 cores 250 MHz on Cortex-M33
	Integer performance	Up to 9000 DMIPS
AI/ML	Ethos™ U-65 microNPU, AI/ML acceleration	Up to 0.5 TOPS
Security Functions	ARM TrustZone®	✓
	Advanced High Assurance Boot	✓
	OTP Fuses and Controller	✓
	Battery Backed Secure Module	✓
	System JTAG controller	✓
	Trusted Resource Domain Controller (TRDC)	✓
	EdgeLock® secure enclave	✓
Memory	LPDDR4 RAM Size	1 GByte, default. Other on request.
	LPDDR4 RAM Speed	3700 MT/s
	LPDDR4 RAM Memory Width	16 bit
	eMMC NAND Flash (8 bit)	8 GByte, default. Other on request.
Graphical Processing	2D/3D Graphics Acceleration	2D Pixel Pipeline (PXP)
Graphical Output	MIPI-DSI, 4 lanes	up to 1920x1200p60 resolution
	LVDS, 4 lanes	up to 1366x768p60 or 1280x800p60
	24-bit parallel RGB	up to 1366x768p60 or 1280x800p60
Graphical Input	MIPI-CSI, 2 lanes	✓ up to 1080p60 resolution
	Image Sensing Interface (ISI), Parallel	✓ 8-bit parallel YUV/RGB
Connectivity Interfaces (all functions are not available at the same time)	2x USB2.0 Type C with Phy	✓
	2x Gigabit Ethernet controllers with support for EEE, Audio Video Bridging (AVB) and IEEE1588. One controller with TSN.	✓ with one on-board Gigabit PHY Second Ethernet interface requires an external Phy.
	2x CAN-FD	✓
	8x SPI, 8x UART, 8x I²C, 2x I³C, 2x FlexIO	✓
	7x I2S TDM, SPDIF, 8-ch PDM, MQS	✓

	2x SD3.0/MMC 5.0	✓ SD1 interface used on-board to eMMC, SD2 interface supports 1.8V/3.3V signaling. SD3 interface fixed at 1.8V (typically used to interface external Wi-Fi/BT module).
	12-bit ADC, 4-channels	✓
	PWMs, WDOG	✓
Other	PMIC (PCA9451AHNY) supporting DVFS techniques for low power modes	✓
	E2PROM storing board information and Ethernet MAC address	✓
	On-board RTC	✓
	On-board watchdog functionality	✓

2.4 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX93 uCOM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX93CEC, i.MX 93 Consumer Application Processors Data Sheet, latest revision
- IMX93IEC, i.MX 93 Industrial Application Processors Data Sheet, latest revision
- IMX93XEC, i.MX 93 Extended Industrial Application Processors Data Sheet, latest revision
- IMX93RM, i.MX 93 Application Processors Reference Manual, latest revision
- IMX93SRM, i.MX 93 Application Processor Security Reference Manual, latest revision
- Chip Errata for the i.MX 93, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN13917, i.MX 93 Power Consumption Measurement, latest revision
- i.MX 93 Product Lifetime Usage, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has defined the EAuCOM board standard with 42 x 45 mm boards that use Hirose DF40C connectors. See the *EAuCOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EAuCOM**.

There are four Hirose DF40C expansion connectors; two 100 pos and two 40 pos connectors. The 0.4mm pitch connectors have a board-to-board stacking height of only 1.5mm. There are also versions of the receptacle connectors that give 3.0mm stacking height.

3.1 Pin Numbering

The figure below illustrates the location of the four expansion connectors and their respective pin numbering on the bottom side of the *iMX93 uCOM Board*.

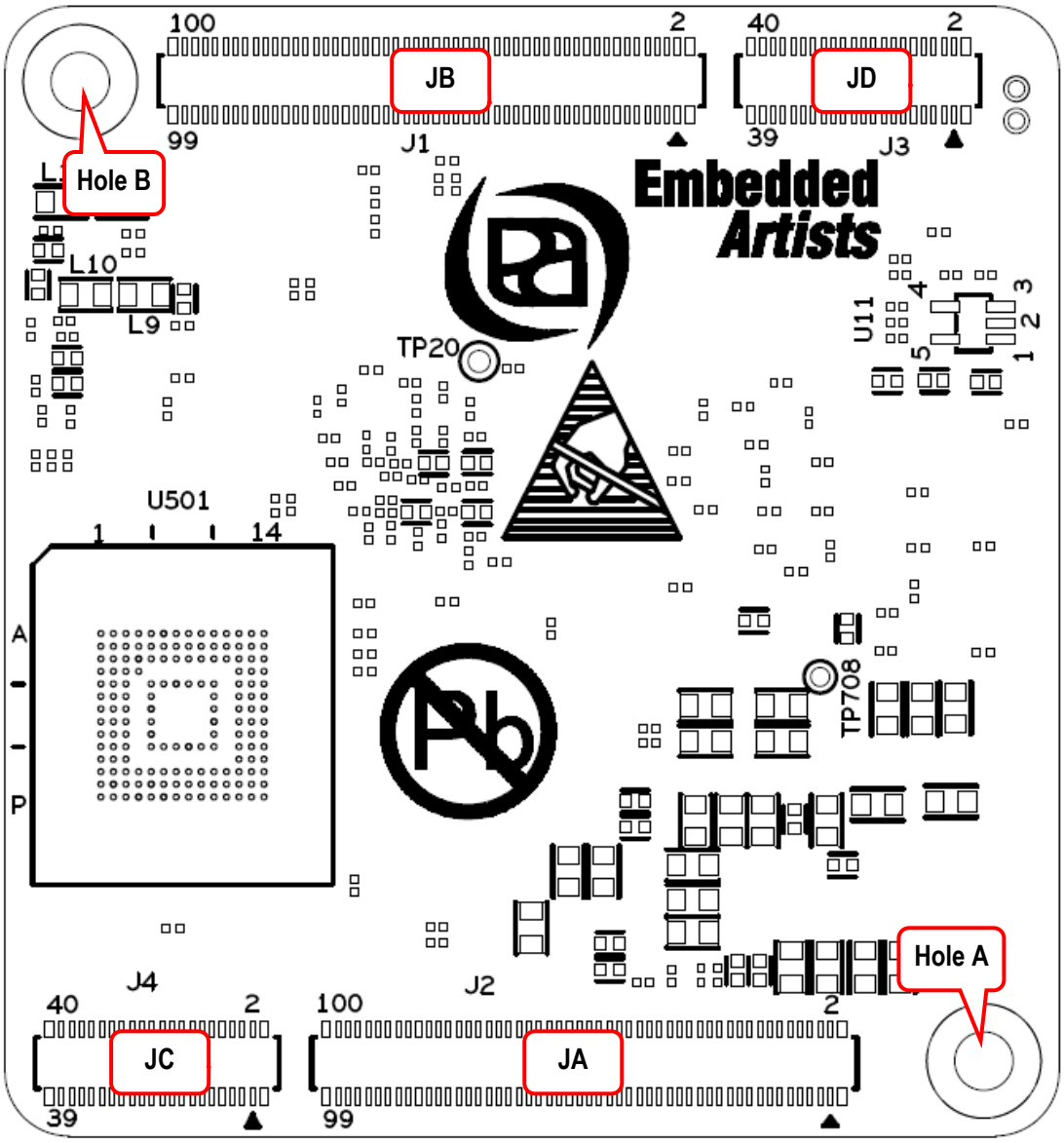

Figure 2 – iMX93 uCOM (EAuCOM standard) Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Connector and Pin number	The pin numbers are listed in consecutive order. Odd pin numbers are on one row and even numbers on the other row.
Non-i.MX 93 signals	Lists signals that are not directly connected to the i.MX 93 SoC. These signals are typically related to powering and connected to the on-board Power Management IC (PMIC), PCA9451AHNY.
i.MX 93 Ball Name	The name of the ball of the i.MX 93 SoC that is connected to this pin.
Alternative Pin Function	Information if the signal is a dedicated interface or a general pin that can multiples different signals. See separate Excel sheet for details about available multiplexing alternatives.
Notes	When relevant, the preferred pin function is listed.

Note that some pins are EAuCOM board *type specific*, meaning that these pins might not be compatible with other EAuCOM boards. Using these may result in lost compatibility between EAuCOM boards, but not always. Check details between EAuCOM boards of interest.

The table below lists the pins on expansion connector JA (100-pos connector).

JA Pin Number	EAuCOM Board Signal	i.MX 93 Ball Name	Alternative Pin Function?	Notes
1-8	VIN_VBAT	PMIC: VSYS_4V2		System supply voltage, see chapter 6 for more details.
9-16	GND			
17	VDD1	PMIC: LDO1 (1.8V NVCC_BBSM_1V8)		Voltage rail, see chapter 6 for more details.
18	VDD_RTC			Not connected. On-board RTC powered via VIN.
19, 21, 23, 25, 27, 29	VDD_1V8	PMIC: BUCK5 (NVCC_1V8)		1.8V voltage rail, see chapter 6 for more details.
20, 22, 24, 26, 28, 30	VDD_3V3	PMIC: BUCK4 (NVCC_3V3)		3.3V voltage rail, see chapter 6 for more details.
31-32	GND			
33	Board specific	GPIO_IO00	Yes	3.3V signaling
34, 36, 38, 40, 42	VDD_RF	-		Not connected
35	Board specific	GPIO_IO03	Yes	3.3V signaling
37	Board specific	GPIO_IO02	Yes	3.3V signaling
39	Board specific	GPIO_IO01	Yes	3.3V signaling
41	GND			
43	Board specific	GPIO_IO04	Yes	3.3V signaling
44	GND			
45	Board specific	GPIO_IO05	Yes	3.3V signaling
46	GND			
47	Board specific	GPIO_IO06	Yes	3.3V signaling
48	VBAT_TEMP	-		Not connected
49	Board specific	GPIO_IO07	Yes	3.3V signaling
50	VBAT_CURRP	-		Not connected

51	GND			
52	VBAT_CURRN	-		Not connected
53	Board specific	GPIO_IO08	Yes	3.3V signaling
54, 56, 58, 60	PSU_5V	-		Not connected
55	Board specific	GPIO_IO09	Yes	3.3V signaling
57	Board specific	GPIO_IO10	Yes	3.3V signaling
59	Board specific	GPIO_IO11	Yes	3.3V signaling
61	GND			
62, 64, 66, 68	VBUS_USB	-		Not connected
63	Board specific	GPIO_IO12	Yes	3.3V signaling
65	Board specific	GPIO_IO13	Yes	3.3V signaling
67	Board specific	GPIO_IO14	Yes	3.3V signaling
69	Board specific	GPIO_IO15	Yes	3.3V signaling
70-71	GND			
72	Board specific	-		Not connected
73	Board specific	GPIO_IO16	Yes	3.3V signaling
74	Board specific	PDM_CLK	Yes	3.3V signaling
75	Board specific	GPIO_IO17	Yes	3.3V signaling
76	Board specific	PDM_DATA0	Yes	3.3V signaling
77	Board specific	GPIO_IO18	Yes	3.3V signaling
78	Board specific	PDM_DATA1	Yes	3.3V signaling
79	Board specific	GPIO_IO19	Yes	3.3V signaling
80	Board specific	I2C-GPIO#2	Yes	Connected to I2C2 GPIO-expander, IO0_2 3.3V signaling
81-82	GND			
83	Board specific	GPIO_IO20	Yes	3.3V signaling
84	Board specific	-		Not connected
85	Board specific	GPIO_IO21	Yes	3.3V signaling
86	Board specific	-		Not connected
87	Board specific	GPIO_IO22	Yes	3.3V signaling
88	Board specific	CLKO04	Yes	**Note**: 1.8V signaling
89	Board specific	GPIO_IO23	Yes	3.3V signaling
90	Board specific	-		Not connected
91-92	GND			
93	Board specific	GPIO_IO24	Yes	3.3V signaling
94	Board specific	-		Not connected
95	Board specific	GPIO_IO25	Yes	3.3V signaling
96	Board specific	-		Not connected
97	Board specific	GPIO_IO26	Yes	3.3V signaling
98	Board specific	TAMPER0	No	**Note**: 1.8V signaling
99	Board specific	GPIO_IO27	Yes	3.3V signaling
100	Board specific	TAMPER1	No	**Note**: 1.8V signaling

The table below lists the pins on expansion connector JB (100-pos connector).

JB Pin Number	EAuCOM Board Signal	i.MX 93 Ball Name	Alternative Pin Function?	Notes
1	UART-C_RXD	-		Not connected
2	GPIO-A	I2C-GPIO#13	Yes	Connected to I2C2 GPIO-expander, IO1_5 3.3V signaling
3	UART-C_TXD	-		Not connected
4	GPIO-B	I2C-GPIO#14	Yes	Connected to I2C2 GPIO-expander, IO1_6 3.3V signaling
5	UART-A_RXD	UART1_RXD	Yes	3.3V signaling
6	GPIO-C	I2C-GPIO#7	Yes	Connected to I2C2 GPIO-expander, IO0_7 3.3V signaling
7	UART-A_TXD	UART1_TXD	Yes	3.3V signaling **Note:** This signal is BOOT_MODE0 and must not be driven externally during powerup/reset. On-board circuit will drive this signal either high or low to control boot source and boot mode. Do not connect any external pull-up or pull-down resistor to this signal.
8	GPIO-D	I2C-GPIO#17	Yes	Connected to I2C2 GPIO-expander, IO2_1 3.3V signaling
9	UART-C_CTS	-		Not connected
10	GPIO-E	I2C-GPIO#4	Yes	Connected to I2C2 GPIO-expander, IO0_4 3.3V signaling
11	UART-C_RTS	-		Not connected
12	GPIO-F	I2C-GPIO#9	Yes	Connected to I2C2 GPIO-expander, IO1_1 3.3V signaling
13	UART-B_RXD	UART2_RXD	Yes	3.3V signaling
14	GPIO-G	I2C-GPIO#23	Yes	Connected to I2C2 GPIO-expander, IO2_7 3.3V signaling
15	UART-B_TXD	UART2_TXD	Yes	3.3V signaling **Note:** This signal is BOOT_MODE1 and must not be driven externally during powerup/reset. On-board circuit will drive this signal either high or low to control boot source and boot mode. Do not connect any external pull-up or pull-down resistor to this signal.
16	GPIO-H	I2C-GPIO#8	Yes	Connected to I2C2 GPIO-expander, IO1_0 3.3V signaling
17	GND			
18	GPIO-J	PMIC_ON_REQ	No	Internal signal between CPU and PMIC. Do not connect to this signal.
19	SD-A_VDD	NVCC_SD2	No	Supply voltage for SD2 interface. Note: this is an output, not an input. No external load except pull-up resistors on the SD2 signals is allowed.
20	GPIO-K	PMIC_STBY_REQ	No	Internal signal between CPU and PMIC. Do not connect to this signal.
21	GND			
22	GPIO-L	SD2_VSEL	No	Internal signal connected to SD2_VSEL, controlling voltage level on SD2 interface (low=3.3V, high=1.8V). Do not connect to this signal. 1.8V signaling
23	SD-A_CLK	SD2_CLK	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)

24	GPIO-M	PMIC: CLK_32K_OUT	No	Connects to PMIC (PCA9451AHNY) CLK_32K_OUT output. Any external load on this signal can affect power consumption on deep-sleep mode.
25	SD-A_CMD	SD2_CMD	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
26	GND			
27	SD-A_DATA0	SD2_DATA0	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
28	SPI-A_SCLK	ADC_IN0	No	**Note**: Analog input. Maximum input voltage is 1.8V
29	SD-A_DATA1	SD2_DATA1	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
30	SPI-A_MISO	ADC_IN1	No	**Note**: Analog input. Maximum input voltage is 1.8V
31	SD-A_DATA2	SD2_DATA2	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
32	SPI-A_MOSI	ADC_IN2	No	**Note**: Analog input. Maximum input voltage is 1.8V
33	SD-A_DATA3	SD2_DATA3	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
34	SPI-A_SS0	ADC_IN3	No	**Note**: Analog input. Maximum input voltage is 1.8V
35	GND			
36	GND			
37	SD-A_WP	-		Not connected
38	SPI-B_SCLK	-		Not connected
39	SD-A_NCD	SD2_NCD	Yes	1.8V/3.3V signaling (depending on SD2_VSEL)
40	SPI-B_MISO	-		Not connected
41	SD-A_NRST	SD2_NRST	Yes	The signal has a 4.7Kohm pull-up resistor to NVCC_SD2. 1.8V/3.3V signaling (depending on SD2_VSEL)
42	SPI-B_MOSI	-		Not connected
43	USB-A_OC	I2C-GPIO#0	Yes	Connected to I2C2 GPIO-expander, IO0_0 3.3V signaling
44	SPI-B_SS0	-		Not connected
45	USB-A_PWR	I2C-GPIO#21	Yes	Connected to I2C2 GPIO-expander, IO2_5 3.3V signaling
46	GND			
47	USB-A_VBUS	USB1_VBUS	No	
48	I2C-A_SCL	I2C1_SCL	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. The signal has an on-board 4.7Kohm pull-up resistor
49	USB-A_DN	USB1_DN	No	
50	I2C-A_SDA	I2C1_SDA	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. The signal has an on-board 4.7Kohm pull-up resistor
51	USB-A_DP	USB1_DP	No	
52	I2C-B_SCL	I2C2_SCL	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. The signal has an on-board 4.7Kohm pull-up resistor
53	USB-A_ID	USB1_ID	No	
54	I2C-B_SDA	I2C2_SDA	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. The signal has an on-board 4.7Kohm pull-up resistor
55	GND			
56	I2C-C_SCL	GPIO_IO29	Yes	Note: this pin does not have an on-board pull-up resistor
57	USB-B_OC	I2C-GPIO#1	Yes	Connected to I2C2 GPIO-expander, IO0_1 3.3V signaling

58	I2C-C_SDA	GPIO_28	Yes	Note: this pin does not have an on-board pull-up resistor
59	USB-B_PWR	I2C-GPIO#22	Yes	Connected to I2C2 GPIO-expander, IO2_6 3.3V signaling
60	I2C-D_SCL	I2C1_SCL	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. This signal is a 1.8V signaling version of I2C1. The signal has an on-board 4.7Kohm pull-up resistor
61	USB-B_VBUS	USB2_VBUS	No	
62	I2C-D_SDA	I2C1_SDA	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board. This signal is a 1.8V signaling version of I2C1. The signal has an on-board 4.7Kohm pull-up resistor
63	USB-B_DN	USB2_DN	No	
64	GND			
65	USB-B_DP	USB2_DP	No	
66	GND			
67	USB-B_ID	USB2_ID	No	
68	PERI_PWR_EN	PMIC: BUCK4 (NVCC_3V3)	No	**Power enable signal for external peripherals. No external must drive any signal to the i.MX 93 SoC before this signal is active.** The signal is active high and is connected to the on-board generate 3.3V supply rail. If all external circuits that can drive a signal to the i.MX 93 SoC are powered from the uCOM-generated 3.3V and 1.8V supplies, this gating signal can be ignored.
69	GND			
70	POR_B	POR_B		Connected to POR_B on the i.MX 93 SoC. Signal shall normally only be used to connect to debug interface connector. Use signals RESET_IN (JB pin 74) to cause a power cycle reset of the board. 1.8V signaling
71	ETH_LED_10/100	ETH_LED_10/100		Connected to on-board Gigabit Ethernet PHY
72	ONOFF	ONOFF		Connected to ONOFF on the i.MX 93 SoC 1.8V signaling
73	ETH_LED_1000	ETH_LED_1000		Connected to on-board Gigabit Ethernet PHY
74	PWRON_B	PMIC: PWRON_B		A falling edge on this input causes a power down of the board. The board will stay in power down for as long as the signal is low. Connect to PMIC (PCA9451AHNY) PWRON_B input.
75	ETH_LED_ACT	ETH_LED_ACT		Connected to on-board Gigabit Ethernet PHY
76	BOOT_MODE0	BOOT_MODE0	No	**This signal shall be left unconnected under normal operation.** The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). This signal is the internal copy of signal UART1_TXD. Note. This signal is 3.3V logic level.
77	GND			
78	BOOT_MODE1	BOOT_MODE1	No	**This signal shall be left unconnected under normal operation.** The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). This signal is the internal copy of signal UART2_TXD. Note. This signal is 3.3V logic level.
79	ETH_TRXP1	ETH_TRXP1		Connected to on-board Gigabit Ethernet PHY

80	TEST_MODE	TEST_MODE		Leave this signal floating (it has an internal 330Kohm pull-up resistor to 3.3V) for booting the Cortex-A55 cores first. This is the default state. Pull signal low to ground to boot the Cortex-M33 core first. Connect this pin to the ground via a zero-ohm resistor. Never directly to ground. This would make it easy to leave the pin floating, if ever needed, by just removing the grounding resistor.
81	ETH_TRXN1	ETH_TRXN1		Connected to on-board Gigabit Ethernet PHY
82	JTAG_VCC	PMIC: BUCK5 (NVCC_1V8)		The supply voltage of the JTAG debug interface, 1.8V. Note that this is not an input. The voltage is provided for reference of the signaling voltage of the JTAG/debug interface.
83	GND			
84	GND			
85	ETH_TRXP0	ETH_TRXP0		Connected to on-board Gigabit Ethernet PHY
86	JTAG_TCK	JTAG_TCK	No	1.8V signaling
87	ETH_TRXN0	ETH_TRXN0		Connected to on-board Gigabit Ethernet PHY
88	JTAG_TMS	JTAG_TMS	No	1.8V signaling
89	GND			
90	JTAG_TDI	JTAG_TDI	No	1.8V signaling
91	ETH_TRXN3	ETH_TRXN3		Connected to on-board Gigabit Ethernet PHY
92	JTAG_TDO	JTAG_TDO	No	1.8V signaling
93	ETH_TRXP3	ETH_TRXP3		Connected to on-board Gigabit Ethernet PHY
94	JTAG_TRST	-		Not connected
95	GND			
96	JTAG_MOD	-		Not connected
97	ETH_TRXN2	ETH_TRXN2		Connected to on-board Gigabit Ethernet PHY
98	BOOT_CTRL			Pull input low to ground to boot based on on-board configuration pullup/pulldown resistors. These resistors configure the boot source to be from the eMMC. **This is the default mode.** Connect this pin to the ground via a zero-ohm resistor. Never directly to ground. This would make it easy to leave the pin floating, if ever needed, by just removing the grounding resistor. Leave floating/open to boot from OTP fuses (on the i.MX 93 SoC). Note that the OTP fuses must first be programmed, typically via UUU. See chapter 5 for more details about boot control and options.
99	ETH_TRXP2	ETH_TRXP2		Connected to on-board Gigabit Ethernet PHY
100	ISP_ENABLE			Leave floating/open for normal boot. Pull low to ground to place i.MX 93 SoC in USB OTG boot mode (during next power cycle). See chapter 5 for more detail about boot control and options.

The table below lists the pins on expansion connector JC (40-pos connector).

JC Pin Number	EAuCOM Board Signal	i.MX 93 Ball Name	Alternative Pin Function?	Notes
1	SD-B_VCC	NVCC_SD3		Supply voltage for SD3 interface, 1.8V. Note: this is an output, not an input. No external load except pull-up resistors on the SD3 signals is allowed.

2	GND			
3	SD-B_CLK	SD3_CLK	Yes	Note: This SDIO signal is fixed at 1.8V signaling
4	Board specific	I2C-GPIO#16	No	Connected to I2C2 GPIO-expander, IO2_0 3.3V signaling
5	SD-B_CMD	SD3_CMD	Yes	Note: This SDIO signal is fixed at 1.8V signaling
6	Board specific	ENET2_MDC	Yes	Note: 1.8V signaling
7	SD-B_DATA0	SD3_DATA0	Yes	Note: This SDIO signal is fixed at 1.8V signaling
8	Board specific	ENET2_MDIO	Yes	Note: 1.8V signaling
9	SD-B_ DATA1	SD3_DATA1	Yes	Note: This SDIO signal is fixed at 1.8V signaling
10	Board specific	ENET2_TD3	Yes	Note: 1.8V signaling
11	SD-B_ DATA2	SD3_DATA2	Yes	Note: This SDIO signal is fixed at 1.8V signaling
12	GND			
13	SD-B_ DATA3	SD3_DATA3	Yes	Note: This SDIO signal is fixed at 1.8V signaling
14	Board specific	ENET2_TD2	Yes	Note: 1.8V signaling
15	Board specific	I2C-GPIO#19	No	Connected to I2C2 GPIO-expander, IO2_3 Output only with 1.8V signaling
16	Board specific	ENET2_TD1	Yes	Note: 1.8V signaling
17	Board specific	I2C-GPIO#18	Yes	Connected to I2C2 GPIO-expander, IO2_2 1.8V signaling via voltage translator. Signal has 10Kohm pull-up resistor to 1.8V
18	Board specific	ENET2_TD0	Yes	Note: 1.8V signaling
19	Board specific	I2C-GPIO#3	Yes	Connected to I2C2 GPIO-expander, IO0_3 1.8V signaling via voltage translator. Signal has 10Kohm pull-up resistor to 1.8V
20	Board specific	ENET2_TX_CTL	Yes	Note: 1.8V signaling
21	Board specific	CLKO01	Yes	Note: 1.8V signaling
22	GND			
23	Board specific	I2C-GPIO#20	No	Connected to I2C2 GPIO-expander, IO2_4 Output only with 1.8V signaling
24	Board specific	ENET2_TXC	Yes	Note: 1.8V signaling
25	Board specific	I2C-GPIO#12	Yes	Connected to I2C2 GPIO-expander, IO1_4 1.8V signaling via voltage translator. Signal has 10Kohm pull-up resistor to 1.8V
26	Board specific	ENET2_RD3	Yes	Note: 1.8V signaling
27	SAI_TXFS	SAI1_TXFS	Yes	3.3V signaling **Note:** This signal is BOOT_MODE2 and must not be driven externally during powerup/reset. An on-chip pull-down resistor will pull this signal low. This is the default state.
28	Board specific	ENET2_RD2	Yes	Note: 1.8V signaling
29	SAI_TXD	SAI1_TXD0	Yes	3.3V signaling **Note:** This signal is BOOT_MODE3 and must not be driven externally during powerup/reset. An on-chip pull-down resistor will pull this signal low. This is the default state.
30	Board specific	ENET2_RD1	Yes	Note: 1.8V signaling
31	SAI_TXC	SAI1_TXC	Yes	3.3V signaling
32	GND			
33	SAI_RXD	SAI1_RXD0	Yes	3.3V signaling
34	Board specific	ENET2_RD0	Yes	Note: 1.8V signaling

35	Board specific	-		Not connected
36	Board specific	ENET2_RX_CTL	Yes	Note: 1.8V signaling
37	Board specific	-		Not connected
38	Board specific	ENET2_RXC	Yes	Note: 1.8V signaling
39	Board specific	I2C-GPIO#10	Yes	Connected to I2C2 GPIO-expander, IO1_2 3.3V signaling
40	Board specific	I2C-GPIO#6	Yes	Connected to I2C2 GPIO-expander, IO0_6 3.3V signaling

The table below lists the pins on expansion connector JD (40-pos connector).

JD Pin Number	EAuCOM Board Signal	i.MX 93 Ball Name	Alternative Pin Function?	Notes
1	DSI_DN3	DSI_DN3	No	
2	CSI_CKN	CSI_CKN	No	
3	DSI_DP3	DSI_DP3	No	
4	CSI_CKP	CSI_CKP	No	
5	GND			
6	GND			
7	DSI_DN0	DSI_DN0	No	
8	CSI_DN0	CSI_DN0	No	
9	SDI_DP0	SDI_DP0	No	
10	CSI_DP0	CSI_DP0	No	
11	GND			
12	GND			
13	DSI_DN2	DSI_DN2	No	
14	CSI_DN1	CSI_DN1	No	
15	DSI_DP2	DSI_DP2	No	
16	CSI_DP1	CSI_DP1	No	
17	GND			
18	GND			
19	DSI_DN1	DSI_DN1	No	
20	CSI_DN2	LVDS_TX3_P	No	
21	DSI_DP1	DSI_DP1	No	
22	CSI_DP2	LVDS_TX3_N	No	
23	GND			
24	GND			
25	DSI_CKN	DSI_CKN	No	
26	CSI_DN3	LVDS_TX2_P	No	
27	DSI_CKP	DSI_CKP	No	
28	CSI_DP3	LVDS_TX2_N	No	
29	GND			
30	GND			
31	Board specific	CLKO03	Yes	**Note**: 1.8V signaling

32	PCIE_RXN	LVDS_CLK_P	No	
33	PCIE_CLKREQ_B	-		Not connected
34	PCIE_RXP	LVDS_CLK_N	No	
35	GND			
36	GND			
37	PCIE_CLKN	LVDS_TX1_P	No	
38	PCIE_TXN	LVDS_TX0_P	No	
39	PCIE_CLKP	LVDS_TX1_N	No	
40	PCIE_TXP	LVDS_TX0_N	No	

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 93 SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to eight different) alternative functions. This leaves great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like MIPI-DSI, MIPI-CSI and USB. i.MX 93 pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between uCOM boards the EAuCOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX93 uCOM Board*. Note that all EAuCOM-defined pins are not connected on some uCOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EAuCOM board pins are *type specific*, meaning that these pins might not be compatible with other uCOM boards. Using *type specific* pins may result in lost compatibility between uCOM boards, but not always. Always check details between uCOM boards of interest.

If switching between uCOM boards is not needed, then pin multiplexing can be done without considering the EAuCOM pin allocation.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 93 pin. For more information about the register settings, see the *i.MX 93 Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings see the *i.MX 93 Application Processor Reference Manual* from NXP.

4.2 Alternative I/O Function List – Work Process

The **i.MX 93 datasheet and reference manuals from NXP shall always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously. There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the EAuCOM function allocation. The reset state is typically the GPIO function, but there are exceptions. It is recommended to study this Excel document to get an overview of the available pin multiplexing options.

The process of defining the pin/function for your system is:

1. Define which interfaces are needed in the system.
2. Allocate each needed interface to either Cortex-A55 ("Linux side") or M33 side ("real-time side").
3. Consult the alternative pin functions Excel sheet and allocate the interfaces to different pins.
    a. If possible, follow the EAuCOM pin and interface allocation. It is not strictly needed but will simplify things if the uCOM board is replaced in a future update/upgrade.
    b. Note that not all signals have 3.3V logic level. Some also have 1.8V logic level.
    c. If pin/function allocation is impossible, the basic architecture under 1) must be reexamined and updated.
4. When a suitable pin/function allocation has been done, update the *.dts file under Linux to enable the interfaces that shall be controlled from the A55/Linux side. On the M33 side, peripherals are enabled and initialized via function calls, see the SDK for details.

4.3 I/O Pin Control

Each GPIO-capable pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `SW_PAD_CTL_PAD_xxx_ddd` where `xxx` is the name of the i.MX 93 pin. For more information about the register settings, see the *i.MX 93 Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, some with pull-down resistor, some without, and some with pull-up resistor, after reset. Some pins are configured as Hi-Z outputs. When the bootloader (typically u-boot) executes it is possible to reconfigure pins.

5 Boot Control

This chapter presents the different boot options/settings that the *iMX93 uCOM Board* supports.

There are four boot control pins that are sampled when the i.MX 93 SoC comes out of reset. These pins are:

- BOOT_MODE0, which is pin UART1_TXD (JB pin 7 with a local copy on JB pin 76)
- BOOT_MODE1, which is pin UART2_TXD (JB pin 15 with a local copy on JB pin 78)
- BOOT_MODE2, which is pin SAI1_TXFS (JC pin 27)
- BOOT_MODE3, which is pin SAI1_TXD0 (JC pin 29) – this pin controls the boot type, see description below

These pins are all outputs if their default functionality is used, so therze is less of a risk an external circuit will drive any of these pins high or low unintentionally (and hence interfere with the boot control).

The *iMX93 uCOM Board* supports booting (i.e., from where the i.MX 93 SoC starts downloading code to start executing from) from different sources:

1. On-board eMMC flash, which is the default, and only boot source supported.
2. USB OTG download (also called 'serial download').
3. Other sources, like external SD/MMC memory cards, SPI flash, etc. This can be controlled by either controlling the BOOT_MODE0..3 pins or by programming the OTP fuses.

There are also two boot types:

- **Single Boot**, which loads all containers and images and then jumps to the Cortex-A55 code.
- **Low-power Boot**, in which only the Cortex-M33 core is running.

The signal TEST_MODE on JB pin 80 controls BOOT_MODE3. When TEST_MODE is floating (which is the default state), BOOT_MODE3 is low, and it results in **Single Boot**. Pull signal TEST_MODE low for **Low-power Boot**.

Signal BOOT_MODE0..2 shall normally not be controlled directly. Instead, there are two signals for controlling the boot source/process, BOOT_CTRL and ISP_ENABLE, see table below:a

Boot source	BOOT_CTRL	ISP_ENABLE
Boot from on-board eMMC Note that the four BOOT_MODE0..3 signals may not be driven externally just after reset by anything other than the slider switches/pull-up resistors because the setting is sampled by the i.MX processor just after reset. This is the default operation for the iMX93 Developer's Kit. **If any of the boot control/configuration signals are driven externally during/just after reset, this mode is not possible. Instead, the on-chip OTP fuses must be programmed to control the boot operation.**	LOW (grounded) Jumper inserted / shorted on carrier board	Floating Jumper open on carrier board
Boot according to OTP fuses (eFuses) • Any boot mode supported by the i.MX 93 SoC and the hardware connected to it can be selected. See *i.MX 93 Applications*	Floating Jumper open on carrier board	Floating Jumper open on carrier board

Processor Reference Manual for details about available sources and OTP fuse settings. • Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to have OTP fuse settings controlling boot source. If not set to 1, the USB OTG boot mode (aka "Serial download") is activated. • Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery. • ***iMX93 uCOM Boards* are delivered without programmed on-chip OTP fuses**. Users have full control over these. • **Note that the only boot source supported is from eMMC.**		
USB OTG This is known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader (typically U-Boot). It is typically not used by the end-product during normal operation. This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.	Do not care	LOW (grounded) Jumper inserted / shorted on carrier board

To summarize:

1. **The iMX93 uCOM board is setup to boot from eMMC mode as default. If another source is needed, program the OTP fuses (see bullet #4 for this).**
   Leave signal ISP_ENABLE floating and BOOT_CTRL grounded for this mode.
2. **If using the default setup (boot from eMMC), make sure the boot control pins (**UART1_TXD (JB pin 7), UART2_TXD (JB pin 15), SAI1_TXFS (JC pin 27), SAI1_TXD0 (JC pin 29)**) are not driven externally during/just after reset.**
   Also, do not connect to JB pin 76 and pin 78 (BOOT_MODE0 and BOOT_MODE1).
3. If signal ISP_ENABLE is pulled low (grounded), the i.MX 93 SoC boots into USB OTG mode. This mode it typically used during development but also during production (when the program images shall be downloaded the first time). **It is recommended to add a feature on the custom carrier board so that pin ISP_ENABLE can be optionally grounded.**
4. To boot from OTP fuses, leave signal BOOT_CTRL floating and program OTP fuses.
5. JB pin 80 (TEST_MODE) should normally be floating for *Single Boot*, i.e., normal Linux booting.

On a custom carrier board, it is recommended to connect signals BOOT_CTRL and TEST_MODE to the ground via separate zero-ohm resistors. Never directly to ground. This would make it easy to leave the pins floating, if ever needed.

5.1 uCOM Carrier Board Boot Control Jumpers

This picture below illustrates where to find the two boot control jumpers on the uCOM Carrier Board.

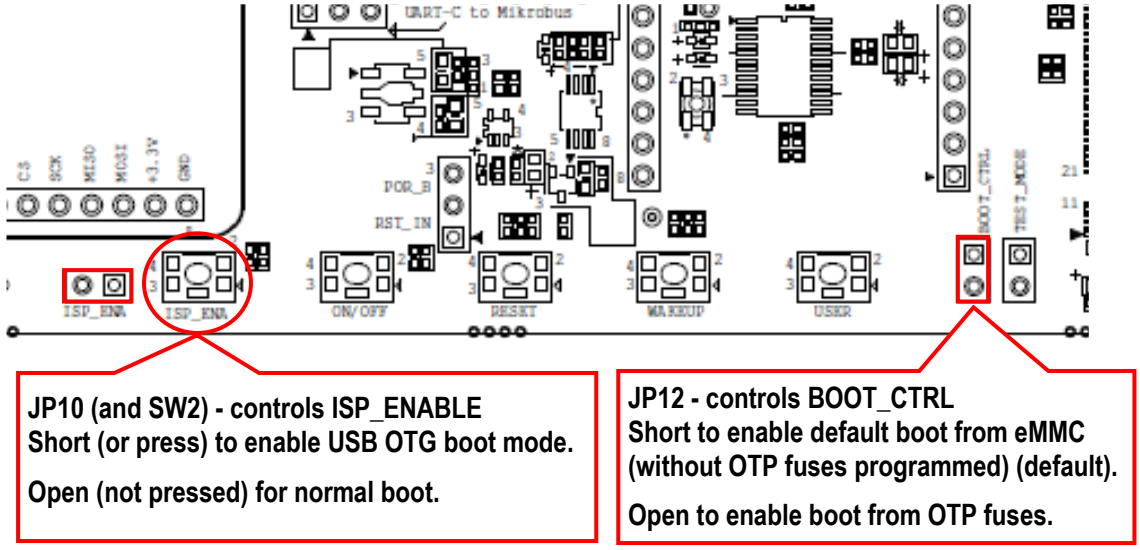

Figure 3 – uCOM Carrier Board, Boot Control Jumpers

6 Powering and PMIC Integration

The i.MX 93 SoC is tightly integrated with the PMIC (PCA9451AHNY) in order to achieve high-performance and low-power operation of the *iMX93 uCOM Board*. The PCA9451AHNY PMIC is specifically developed for the i.MX 93 SoC. It also includes a real-time clock. See the PCA9451AHNYdatasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are also available for the carrier board design, reducing integration cost. Designs with moderate power consumption may not need any external power supply at all. Everything can be handled by the on-board PMIC.

6.1 Available Power Supply Rails

The table below presents the available power rails that can be used on the carrier board that the *iMX93 uCOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
NVCC_3V3 **on JA pins 20/22/24/26/28/30**	3.3V for external use on carrier board.	3.3V	400mA
NVCC_1V8 **on JA pins 19/21/23/25/27/29**	1.8V for external use on carrier board.	1.8V	400mA

Note that each pin on the Hirose DF40C expansion connectors can carry 300mA maximum. Connect to all pins on the expansion connectors that carry a specific power rail. High current power rails have more than one pin.

Note that external load variations can affect the PMIC operation and potentially disturb the i.MX 93 SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails. Also **calculate the heat dissipation** of the PMIC in case the carrier board has high current consumption.

6.2 Integration

This integration is very simple. An external 3.5-5.5V supply is all that is needed. The internal RTC is powered by this supply also, i.e., there is no separate RTC supply input.

- Supply the 3.5-5.5V input voltage to **VSYS_4V2** (connect to all eight pins on connector JA)
- Leave signals VBAT_RTC_IN. BAT_TEMP, BAT_CURRP and BAT_CURRN unconnected.
- Leave supply inputs PSU_5V on JA pin 54/56/58/60 and VBUS_USB on JA pin 62/64/66/68 unconnected.

7 Technical Specification

7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VSYS_4V2	Main input supply voltage	-0.3	5.5	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO	0	3.6	V
	Vin/Vout (I/O VDD + 0.3): 1.8V IO	0	1.98	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VSYS_4V2	Main input supply voltage	3.5		5.5	V
	Ripple with frequency content < 10 MHz			50	mV
	Ripple with frequency content ≥ 10 MHz			10	mV
USB_xx_VBUS	USB VBUS signals		5	5.25	V

7.3 Power Ramp-Up Time Requirements

The input supply voltage (VSYS_4V2) shall have a smooth and continuous ramp from 10% to 90% of final set-point. The input supply voltage shall reach the recommended operating range in 1-20 ms.

7.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see i.MX 93 Datasheet. The internal VDD operating point for GPIOs is 3.3V or 1.8V for all signals.

7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN. Maximum output voltage when active is 0.4V.

7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 10 uS minimum. The internal reset pulse will be about 250 mS long, before the i.MX 93 boot process starts.

7.5 Power Consumption

There are several factors that determine power consumption of the *iMX93 uCOM Board*, like input voltage, operating temperature, LPDDR4 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

Symbol	Description (VIN = 4.2V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 1.7 GHz ARM frequency, without Ethernet		TBD	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt		TBD TBD	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA

7.6 Mechanical Dimensions

The table below presents the mechanical dimensions of the module.

Dimension	Value (±0.1 mm)	Unit
Module width	42	mm
Module height	45	mm
Module top side height	2.0	mm
Module bottom side height	1.4	mm
PCB thickness	1.4	mm
Mounting hole diameter	2.3	mm
Module weight	2 ±0.5 gram	gram

The picture below illustrates the mechanical details of the *iMX93 uCOM Board*. The outer measurement is 42 x 45 mm. Note that the picture is seen from the bottom side.

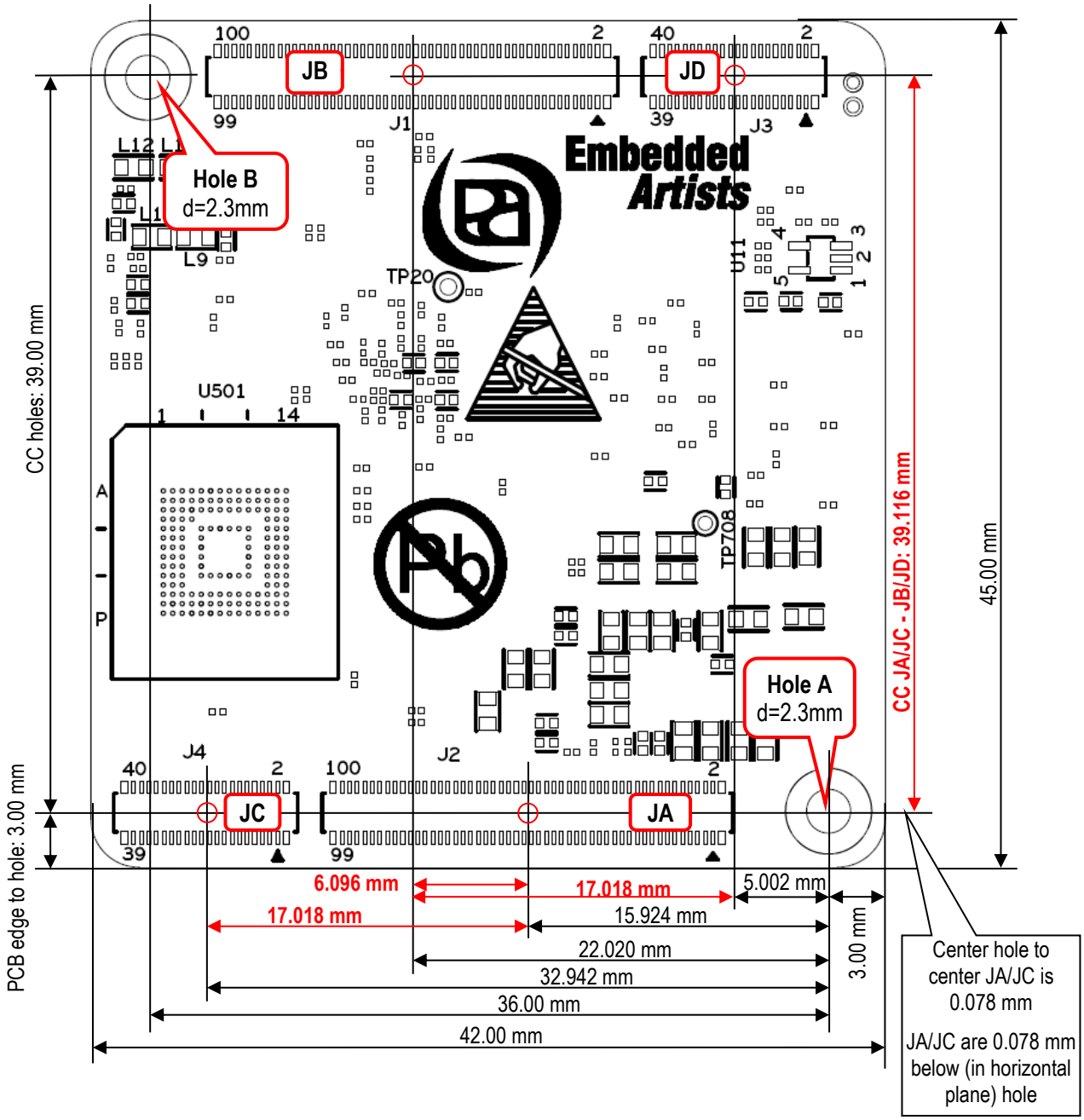

Figure 4 – iMX93 uCOM Board Mechanical Outline, View from Bottom Side

Note that placement of the connectors on the carrier board is very important. They must be parallel and have a placement tolerance of +-0.1mm (non-accumulative). Make sure the relative measures between the connectors (marked with red in the picture above) are correct.

Note that the mounting hole location shall be measured relative to the three connectors, not relative to the pcb edge.

Since the stacking height is only 1.5mm in normal case, make sure no components other than the three connectors are within the dotted red line. When using 3mm stacking height it is possible to have low-profile components under the *iMX93 uCOM Board*. The picture below illustrates the principal dimensions.

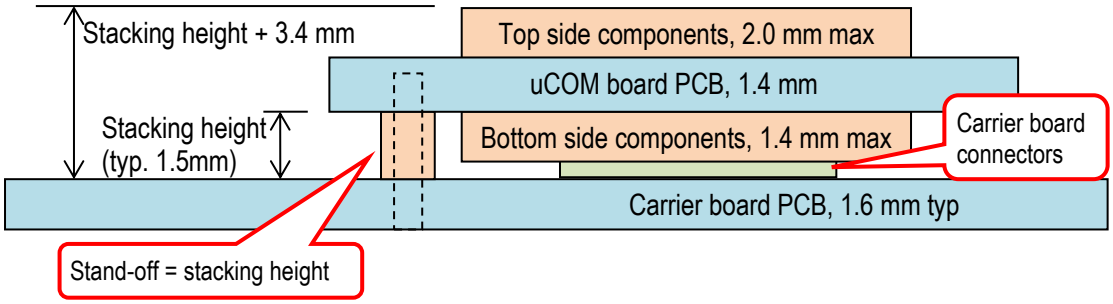

Figure 5 – uCOM Board Mounting on Carrier Board, Stacking Height

7.6.1 DF40C Socket

The headers mounted on the *iMX93 uCOM Board* are DF40C-100DP-0.4V(51) (for JA / JB) and DF40C-40DP-0.4V(51) (for JC / JD).

The receptacles that are needed on the carrier board are, depending on stacking height:

Connector	1.5 mm stacking height (standard)	3.0 mm stacking height
100-pos (JA / JB)	DF40C-100DS-0.4V(51) HRS number: 684-4033-4 51	DF40HC(3.0)-100DS-0.4V(51) HRS number: 684-4151-0 51
40-pos (JC / JD)	DF40C-40DS-0.4V(51) HRS number: 684-4008-7 51	DF40HC(3.0)-40DS-0.4V(51) HRS number: 684-4169-6 51

If any of the connectors are not needed on the carrier board design, these do not have to be mounted. This typically applies to JC and JD.

7.6.2 Module Assembly Hardware

The *iMX93 uCOM Board* has two 2.3mm mounting holes for securing a good mechanical mounting. Use M2 screws and associated standoffs that have the same height as the stacking height (1.5mm or 3 mm, depending on carrier board connectors).

When mounting the iMX93 uCOM board, match hole A on the carrier board with hole A on the uCOM board before the final mounting.

7.7 Environmental Specification

7.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter	Min	Max	Unit
Operating temperature range: extended temperature range	-25	85[1]	°C
Storage temperature range	-40	85	°C

Junction temperature i.MX 93 SoC, operating:	ext. temp. range.	-40	105	°C

[1] Depends on cooling/heat management solution.

7.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: -25°C ≤ T_A ≤ 85°C, non-condensing (ext. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

7.8 Thermal Design Considerations

Heat dissipation from the i.MX 93 SoC depends on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat can be up to 3 Watt but is typically much lower.

Whether external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *iMX93 uCOM Board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 93 SoC.

The i.MX 93 SoC implements DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling via the Linux BSP. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general, this results in higher performance at lower average power consumption.

The i.MX 93 SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affects several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: i.MX 93 Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

7.8.1 Thermal Parameters

The i.MX 93 SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	22.9	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	4	°C/W

7.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

8 Functional Verification and RMA

There is a separate document that presents several functional tests that can be performed on the *iMX93 uCOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX93 uCOM Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

9 Things to Note

This chapter presents a number of issues and considerations that users must note.

9.1 Shared Pins and Multiplexing

The i.MX 93 SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX93 uCOM* on-board design. Check if the needed interfaces are available to allocation before starting a design. See chapter 4 for details.

9.2 Only Use EA Board Support Package (BSP)

The *iMX93 uCOM board* uses multiple on-board interfaces for the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX93 uCOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

9.3 OTP Fuse Programming

The i.MX 93 SoC has on-chip OTP fuses that can be programmed, see NXP documents *i.MX 93 Datasheet* and *iMX 93 Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX93 uCOM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses should be programmed and, in that case, which ones.

Note that Embedded Artists does not replace iMX93 uCOM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

9.4 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write-protected if signal ISP_ENABLE JB pin 100 on DF40C connector is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the i.MX 93 SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

9.5 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- iMX Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX93 uCOM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Building Safety / Security
- Home appliances
- Robotic appliance
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll / Ticketing Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX93 uCOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX93 uCOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX93 uCOM Board*.

9.6 ESD Precaution when handling iMX93 uCOM Board

Please note that the *iMX93 uCOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

9.7 EMC / ESD

The *iMX93 uCOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless, depending on the target system, additional anti-interference measurement may still be necessary to adhere to the limits for the overall system.

The *iMX93 uCOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only make sense on the complete solution.

No specific ESD protection has been implemented on the *iMX93 uCOM Board*. ESD protection on board level is the same as what is specified in the i.MX 93 SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

10 Custom Design

This document specifies the standard *iMX93 uCOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Mounting a Wi-Fi/BT module.
- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on DF40C connectors.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *iMX93 uCOM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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