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Page 4:	Push-buttons and Boot control
Page 5:	I2C GPIO Expander and user LEDs and button
Page 6:	JTAG Debug Interface and Optional QSPI
Page 7:	Parallel LCD interface
Page 8:	Optional Boot Control Pins
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Page 11:	Camera Interface
Page 12:	Ethernet Interface for on-board PHY
Page 13:	USB OTG and USB C Interface
Page 14:	USB Host Interface and Hub
Page 15:	UART-to-USB bridge interfaces
Page 16:	Mikrobus/Click Module Interface
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UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic.
However, always check jumper positions on actual boards
since there is no guarantee that all jumpers are in default place.

Rev B

Added R311/R312 and JP35. Delete R152.
Delete Q24, added D39/D41/D42. Added U30.
Delete U38/U39, added U40/U41.
Delete D7/U2, added Q29/Q30.
Delete JP8/JP9, add J14 and J38. Change J15.
Adding SPI support for the M.2 E-key connector.

Rev PB3

Replace D35 with U38 and D36 with U39.
Updated LED driving of J25. Update U36 package.
Updated current measurements (JP4-JP7/JP29/JP34/JP43)

Rev PB1-PB2

Removed one camera interface.
Separate power supply to M.2 interfaces.
Replaced MIPI-to-LVDS bridge with new design.

Rev A

First release



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TITLE: uCOM Carrier board rev B

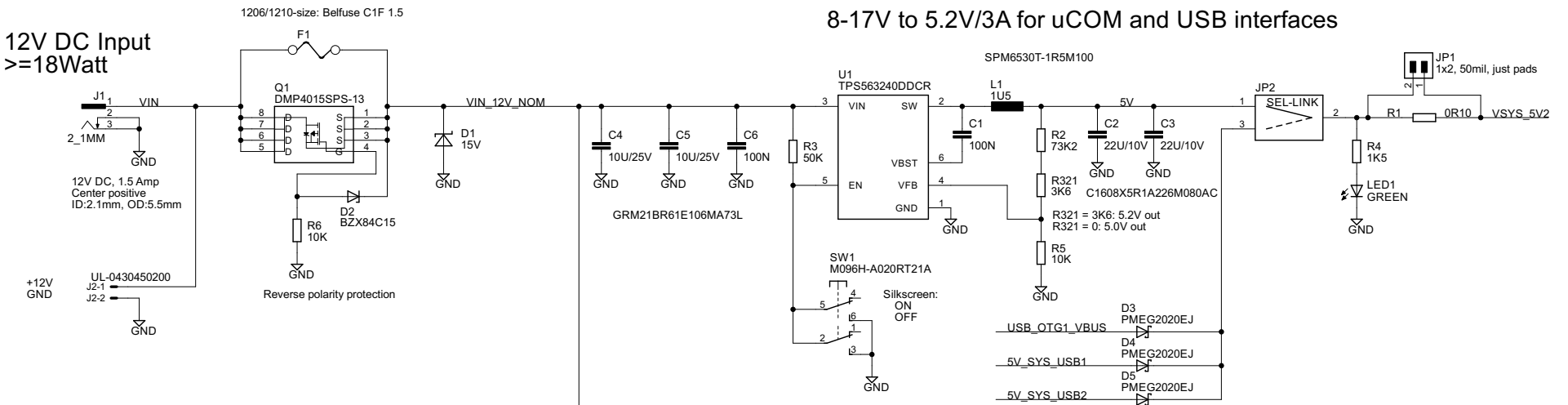
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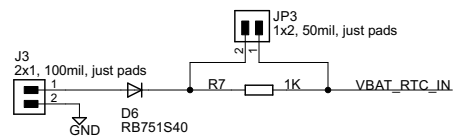
Sheet: 1/25

Powering

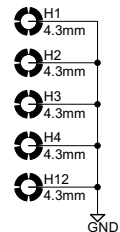
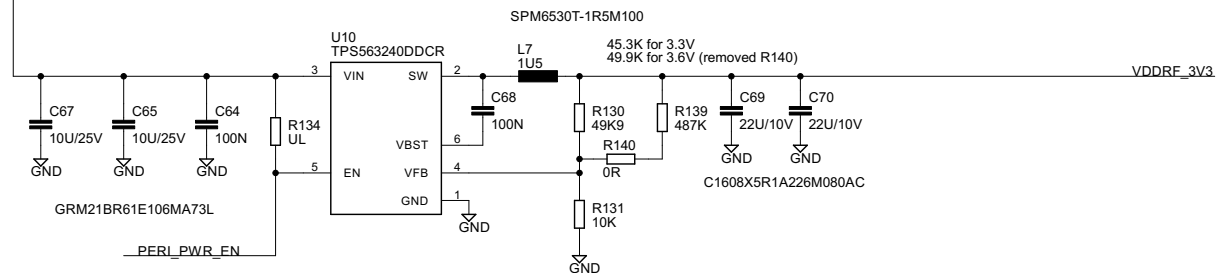
12V DC Input
 >=18Watt



VBAT input



8-17V to 3.3V/3A for M.2 interfaces (wireless modules)



GND connectors
(Keystone 5016K)



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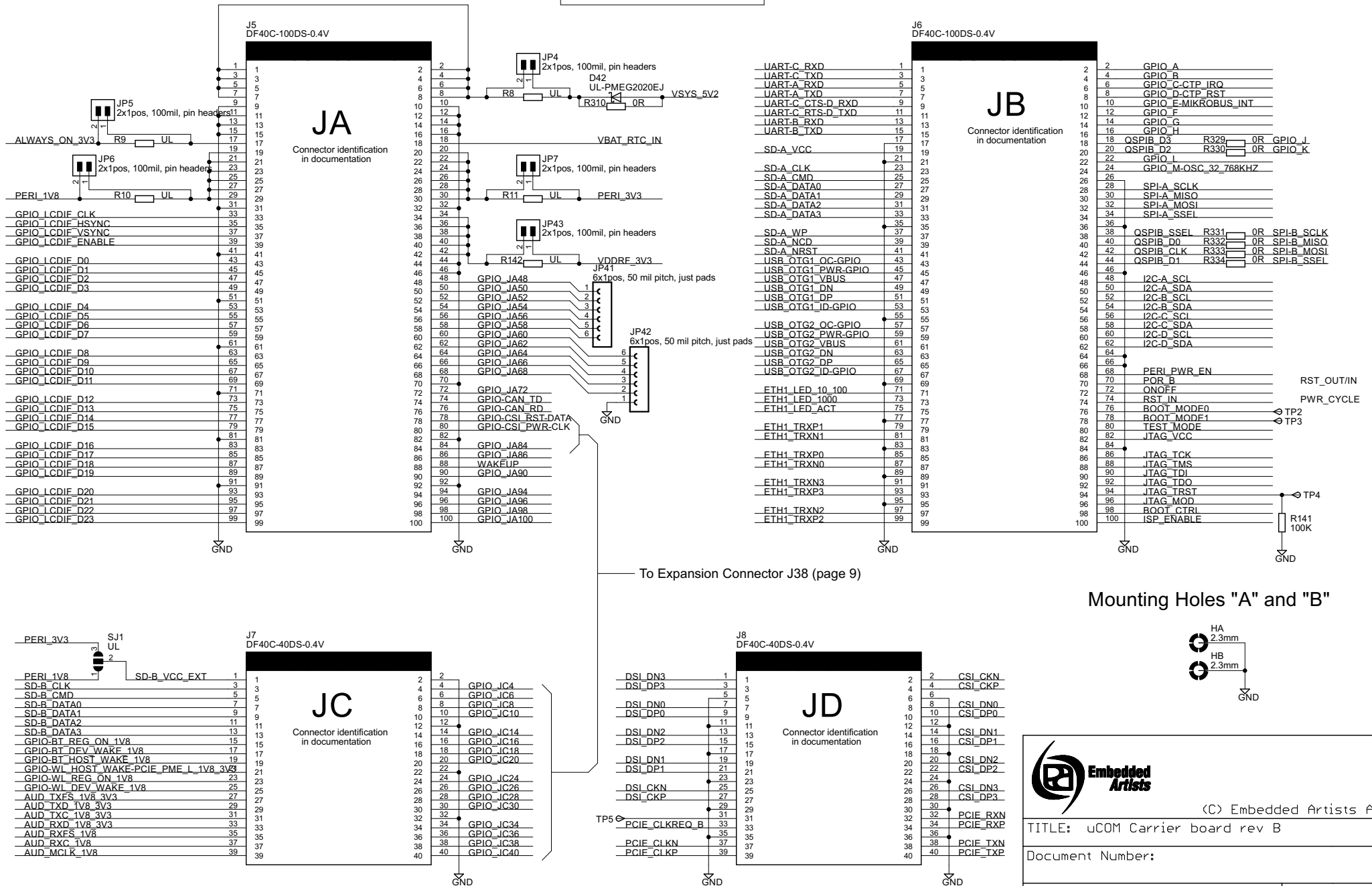
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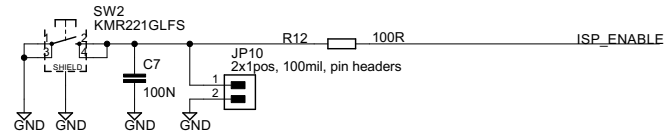
Sheet: 2/25

uCOM Connectors

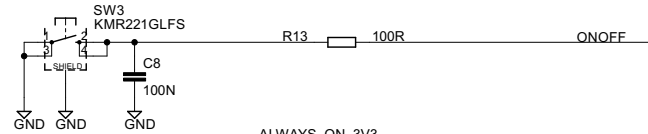


Push-buttons and Boot control

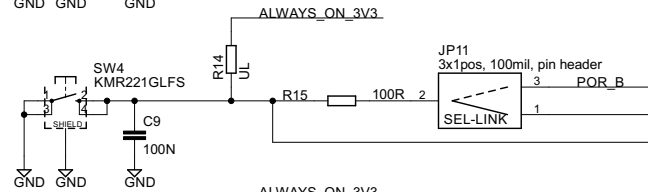
ISP Enable push-button and jumper



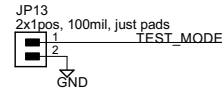
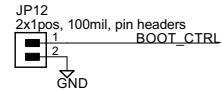
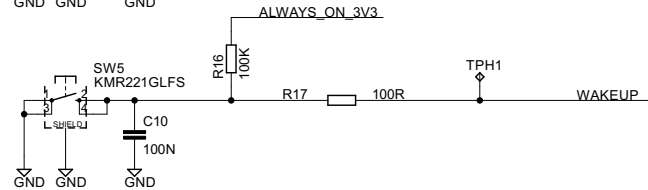
ONOFF push-button



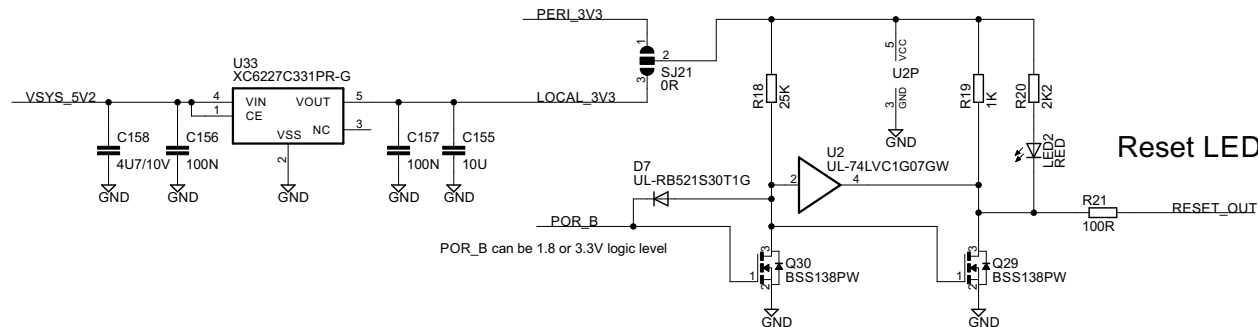
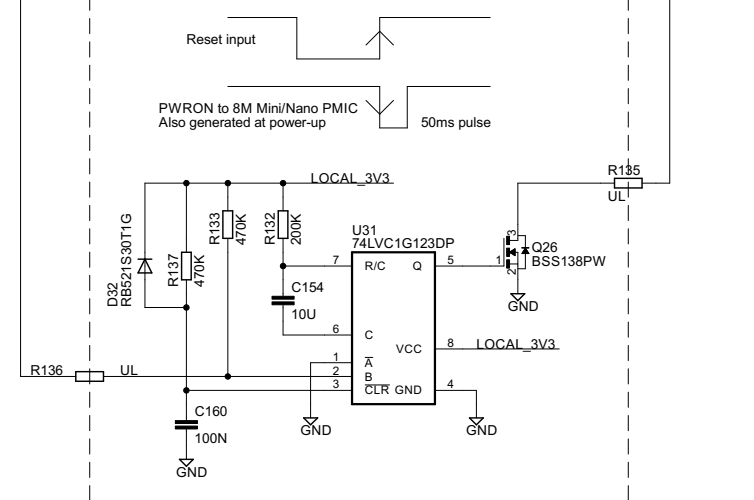
Reset push-button



Wakeup push-button



Optional control for iMX8M Mini/Nano



Reset LED



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TITLE: uCOM Carrier board rev B

Document Number:

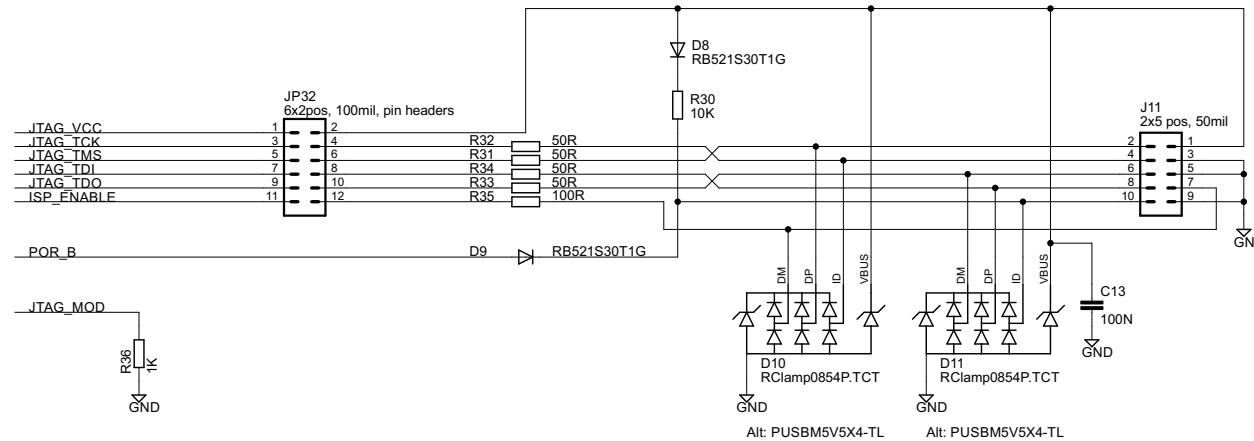
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Sheet: 4/25

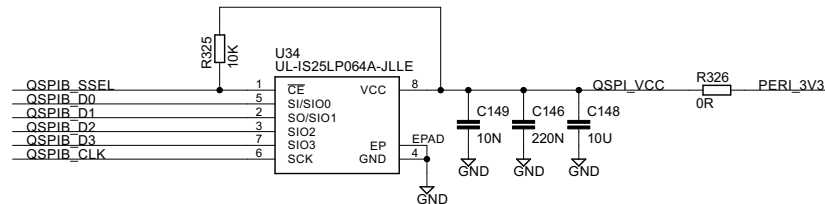
JTAG Debug Interface and Optional QSPI

Special option for i.MX93 platform

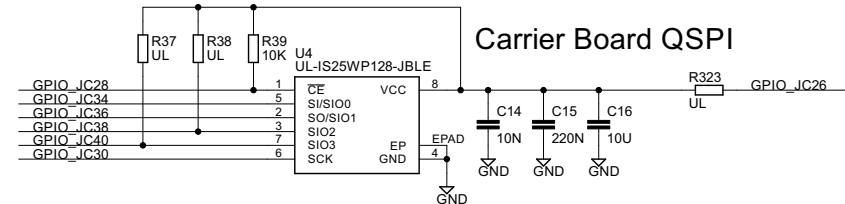
Open jumpers to access UART channel (for M.2 UART interface).
It is possible to connect secondary JTAG interface from GPIO_LCDIF_20-GPIO_LCDIF_23.



Pads for carrier board QSPI (for iMX RT1064 uCOM)



Pads for carrier board QSPI (for iMX8M Mini/Nano uCOM)



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TITLE: uCOM Carrier board rev B

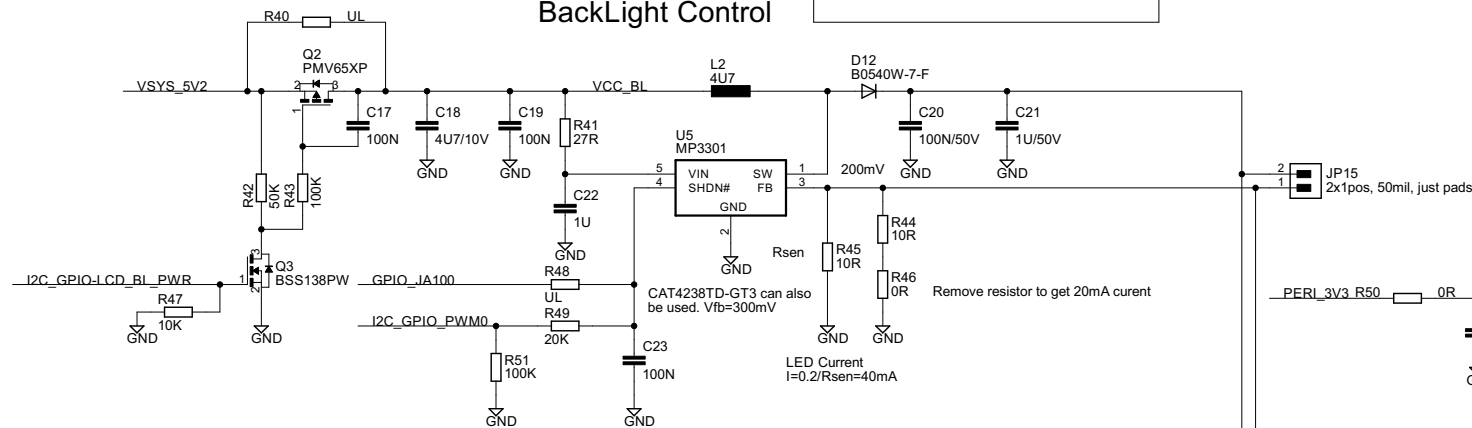
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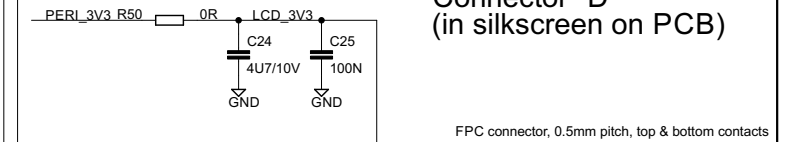
Sheet: 6/25

Parallel LCD interface

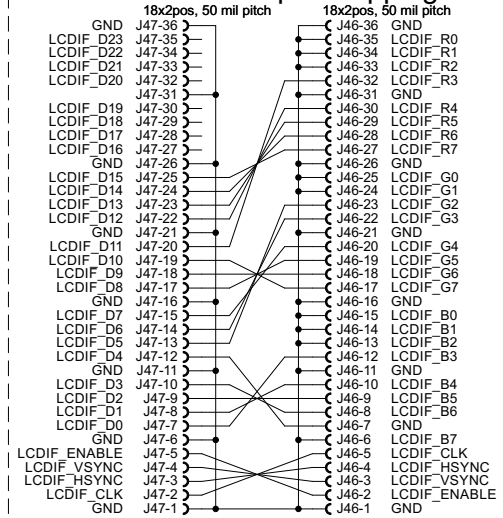
BackLight Control



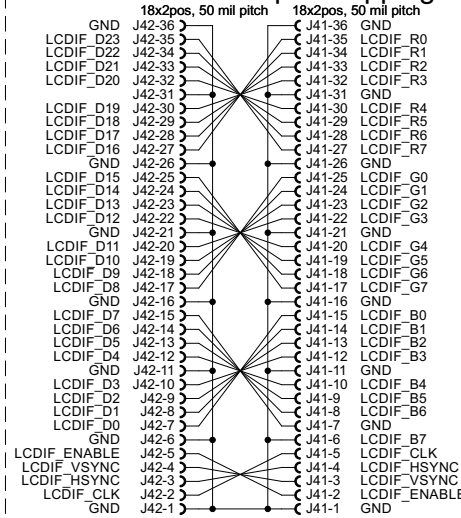
Common Parallel RGB Display pinning Connector "D" (in silkscreen on PCB)



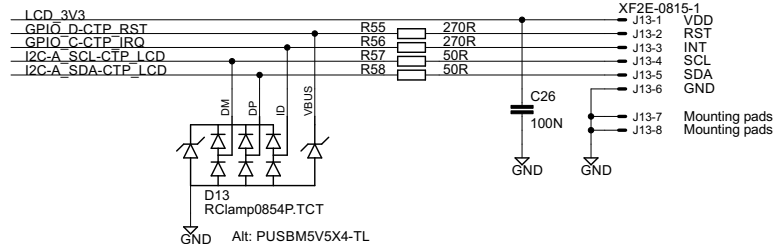
16-bit color depth mapping



24-bit color depth mapping

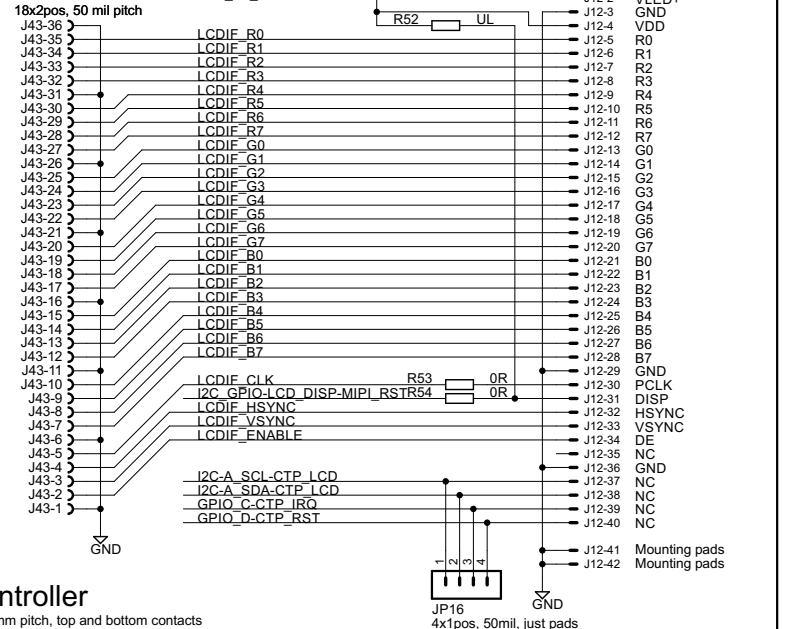


Mapping for external 100Mbps Ethernet



Touch controller

FPC connector, 0.5mm pitch, top and bottom contacts



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TITLE: uCOM Carrier board rev B

Document Number:

Date: not saved!

Sheet: 7/25

Optional Boot Control Pins

JA pin 33 (GPIO_LCDIF_CLK)
JA pin 35 (GPIO_LCDIF_HSYNC)
JA pin 37 (GPIO_LCDIF_VSYNC)
JA pin 39 (GPIO_LCDIF_ENABLE)

JA pin 43 (GPIO_LCDIF_D0)
JA pin 45 (GPIO_LCDIF_D1)
JA pin 47 (GPIO_LCDIF_D2)
JA pin 49 (GPIO_LCDIF_D3)

JA pin 53 (GPIO_LCDIF_D4)
JA pin 55 (GPIO_LCDIF_D5)
JA pin 57 (GPIO_LCDIF_D6)
JA pin 59 (GPIO_LCDIF_D7)

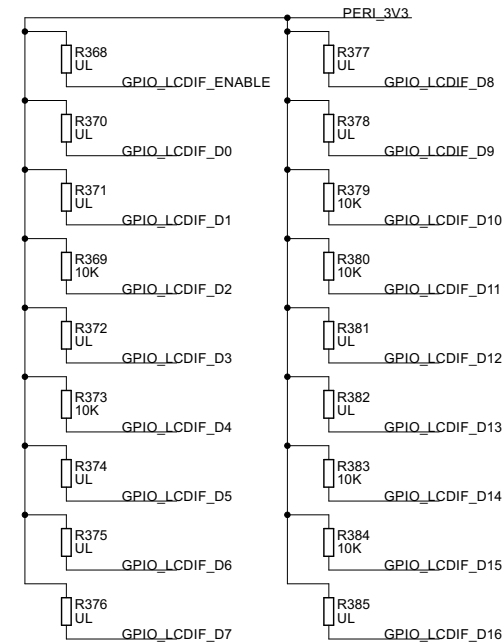
JA pin 63 (GPIO_LCDIF_D8)
JA pin 65 (GPIO_LCDIF_D9)
JA pin 67 (GPIO_LCDIF_D10)
JA pin 69 (GPIO_LCDIF_D11)

JA pin 73 (GPIO_LCDIF_D12)
JA pin 75 (GPIO_LCDIF_D13)
JA pin 77 (GPIO_LCDIF_D14)
JA pin 79 (GPIO_LCDIF_D15)

JA pin 83 (GPIO_LCDIF_D16)
JA pin 85 (GPIO_LCDIF_D17)

iMX8M Mini	RT1064	RT1176
SAI1_TXD0 BT_CFG8-0	MDC MDIO	
SAI1_TXD1 BT_CFG9-0	BT_CFG10	BT_CFG0
SAI1_TXD2 BT_CFG10-0	BT_CFG11	BT_CFG1
SAI1_TXD3 BT_CFG11-1	BT_CFG12	
SAI1_TXD4 BT_CFG12-0	BT_CFG13	
SAI1_TXD5 BT_CFG13-1	BT_CFG14	BT_CFG2
SAI1_TXD6 BT_CFG14-0	BT_CFG15	BT_CFG3
SAI1_TXD7 BT_CFG15-0	BT_CFG16	BT_CFG4
	BT_CFG17	BT_CFG5
SAI1_RXD0 BT_CFG0-0	TX0 BT_CFG20	BT_CFG6
SAI1_RXD1 BT_CFG1-1	TX1 BT_CFG21	BT_CFG7
SAI1_RXD2 BT_CFG2-1	TX_EN BT_CFG22	BT_CFG8
	TX_CLK BT_CFG23	BT_CFG9
SAI1_RXD3 BT_CFG3-0	RX_ER	BT_CFG10
SAI1_RXD4 BT_CFG4-0	RX0	BT_CFG11
SAI1_RXD5 BT_CFG5-1	RX1	
SAI1_RXD6 BT_CFG6-1	RX_EN	
SAI1_RXD7 BT_CFG7-0		RX_EN
		RX_ER

Support access to boot control signals (default set for iMX8M Mini booting from eMMC)



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TITLE: uCOM Carrier board rev B

Document Number:

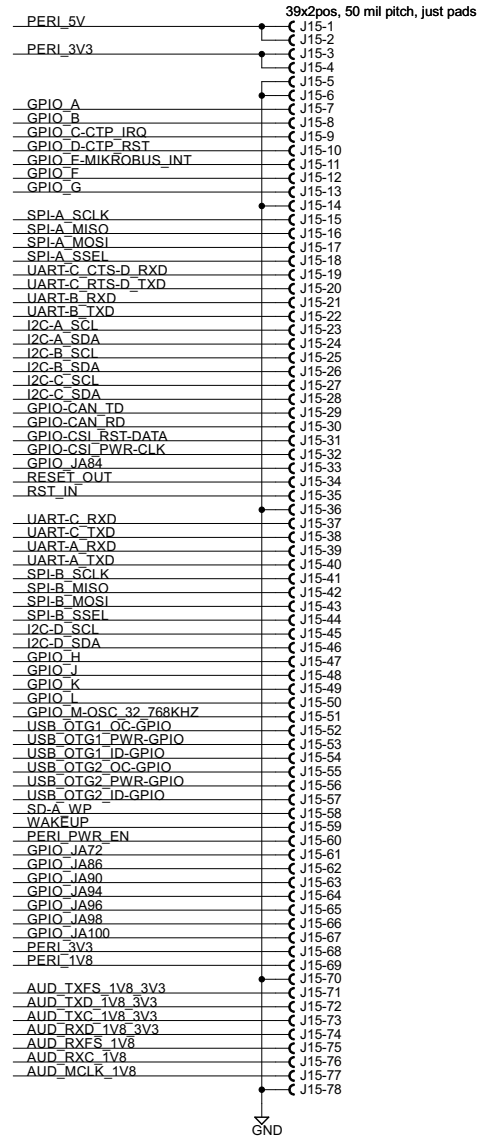
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Sheet: 8/25

Expansion Connectors

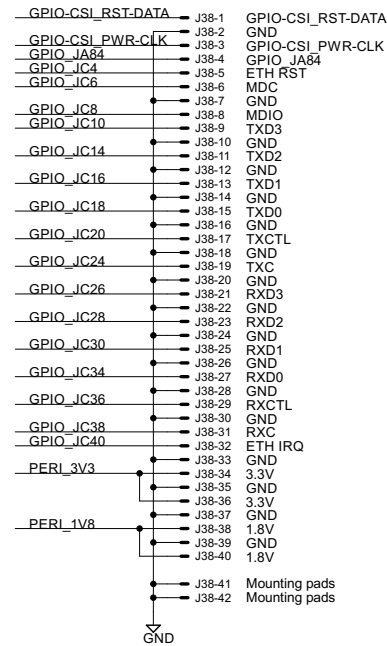
Connector "A" (in silkscreen on PCB)

2x39-pos 50 mil pitch matrix



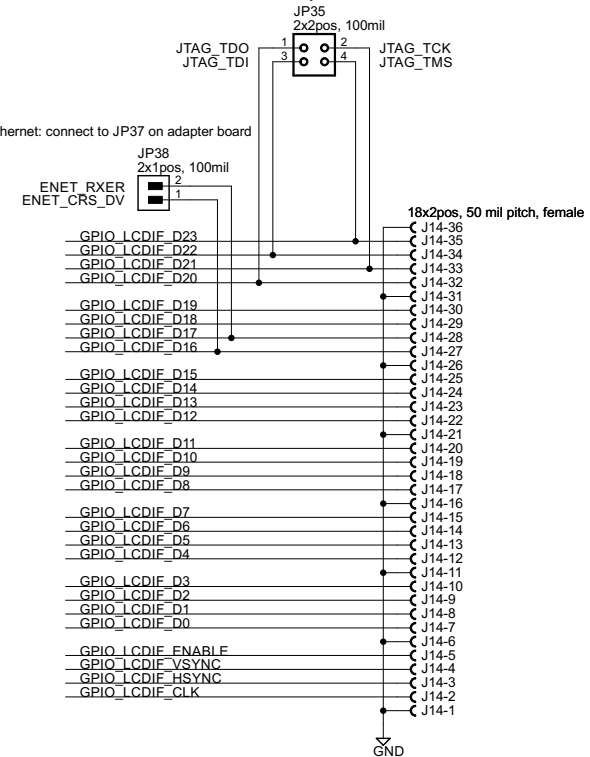
Connector "E" (in silkscreen on PCB)

0.5mm pitch, top and bottom contacts
XF2W-4015-1A or 68714014022



Connector "B" 2x18-pos 50 mil pitch matrix

For iMX93 secondary JTAG interface: connect to JP32



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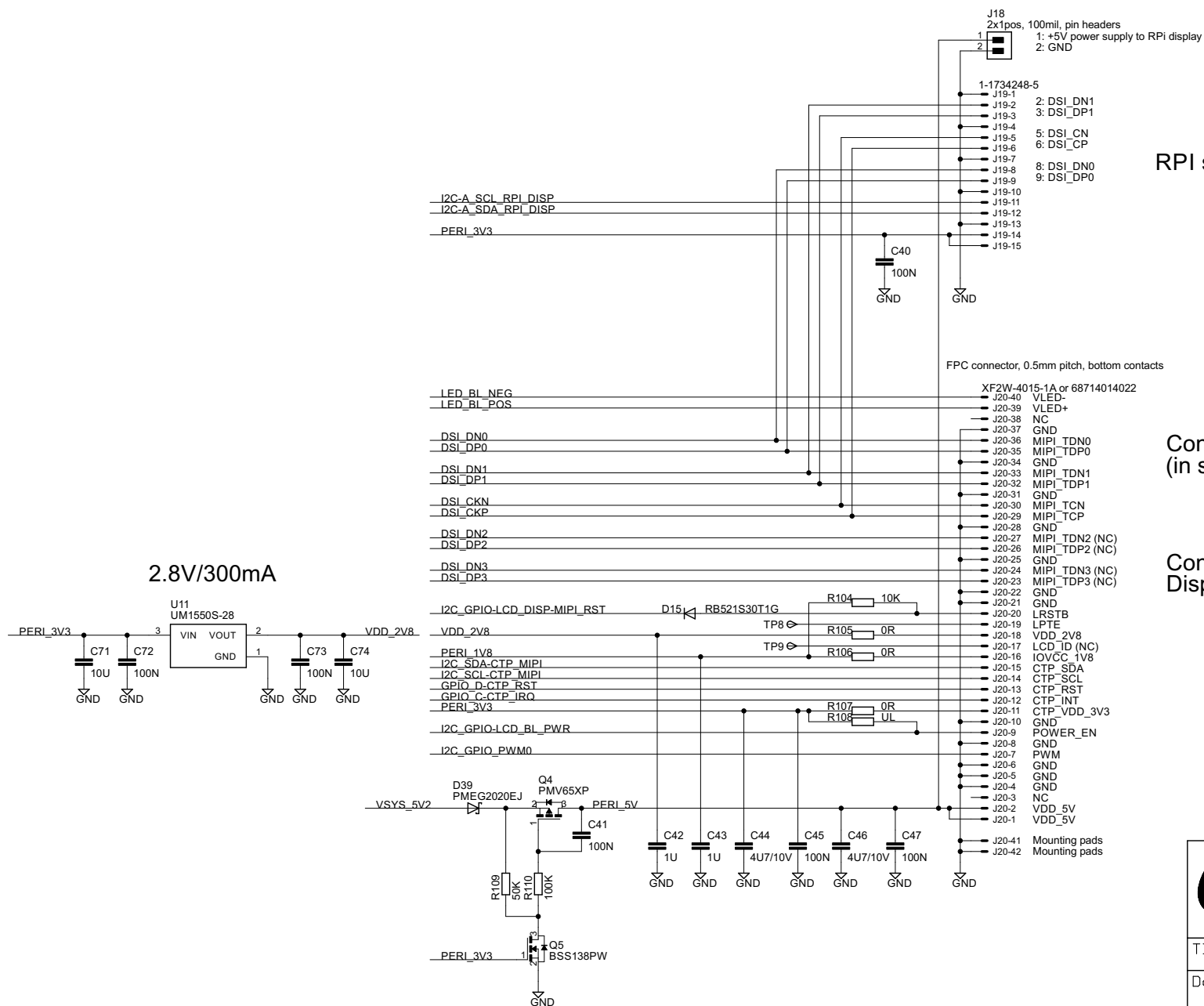
TITLE: uCOM Carrier board rev B

Document Number:

Date: not saved!

Sheet: 9/25

MIPI-DSI Display Interfaces



RPI serial display (MIPI)

Connector "C"
(in silkscreen on PCB)

Connects to NXP RK055HDMIPI4M
Display: RK055AHD091-CTG(720P)



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TITLE: uCOM Carrier board rev B

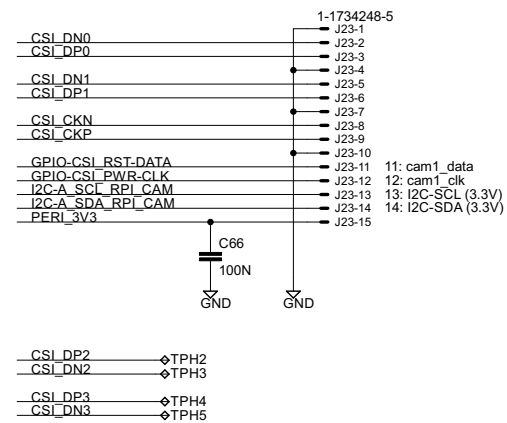
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Sheet: 10/25

Camera Interface

RPI serial camera (MIPI)



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TITLE: uCOM Carrier board rev B

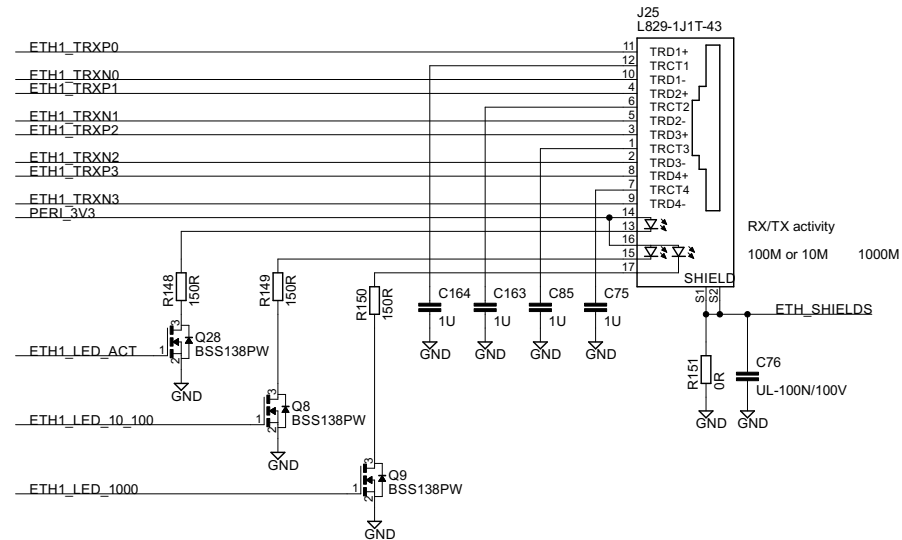
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Sheet: 11/25

Ethernet Interface for on-board PHY

Ethernet Interface



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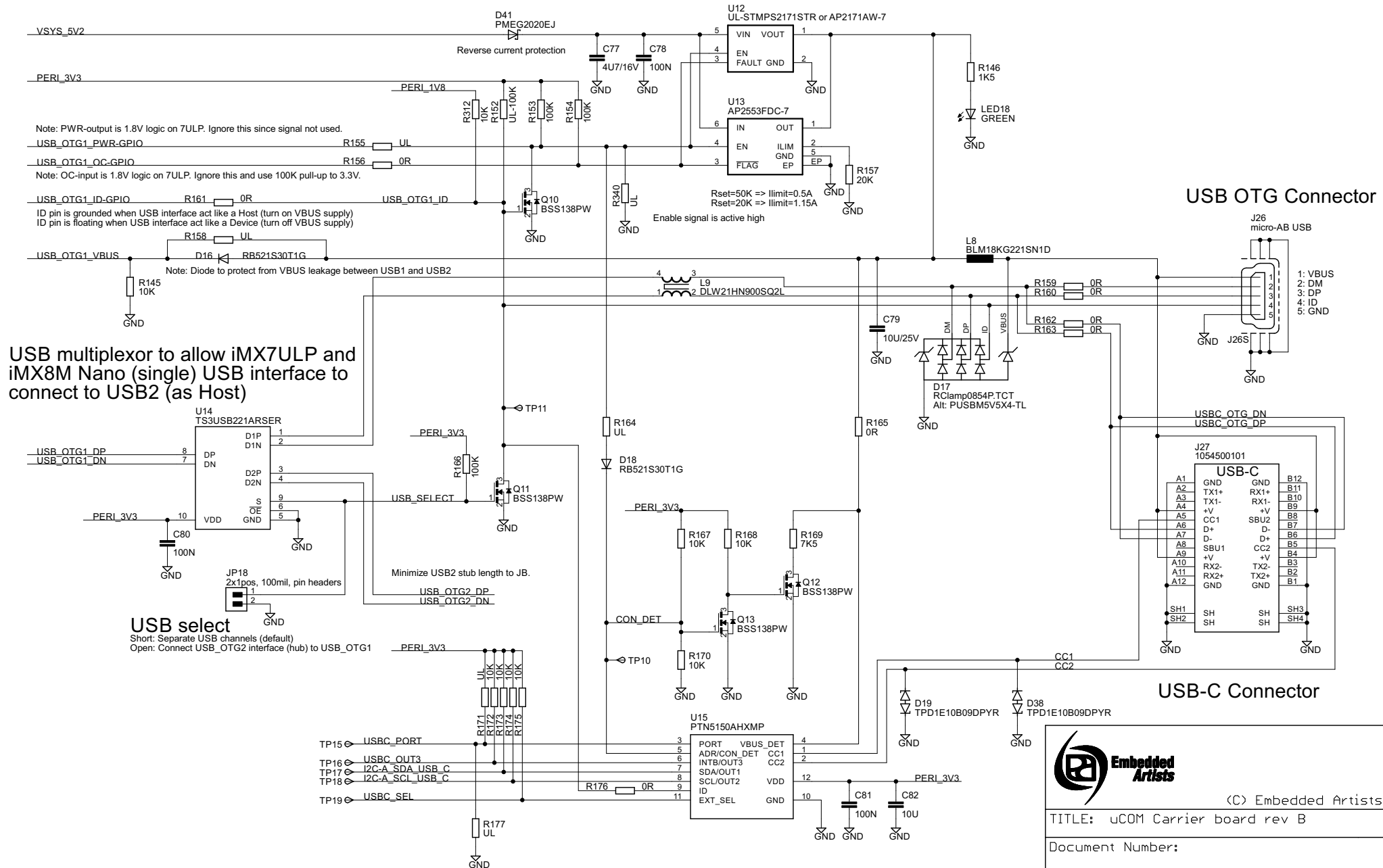
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Sheet: 12/25

USB OTG and USB C Interface



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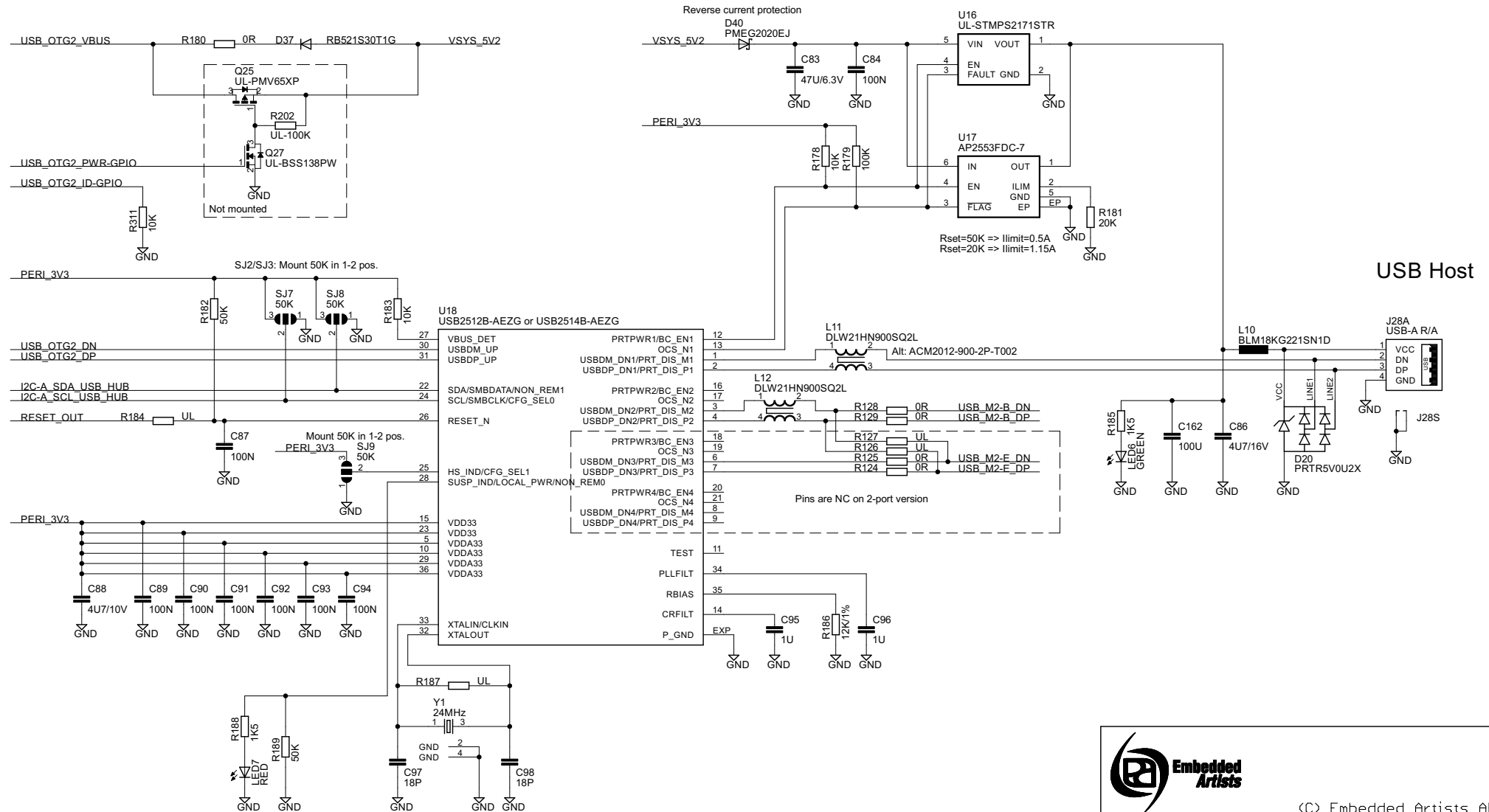
TITLE: uCOM Carrier board rev B

Document Number:

Date: not saved!

Sheet: 13/25

USB Host Interface and Hub



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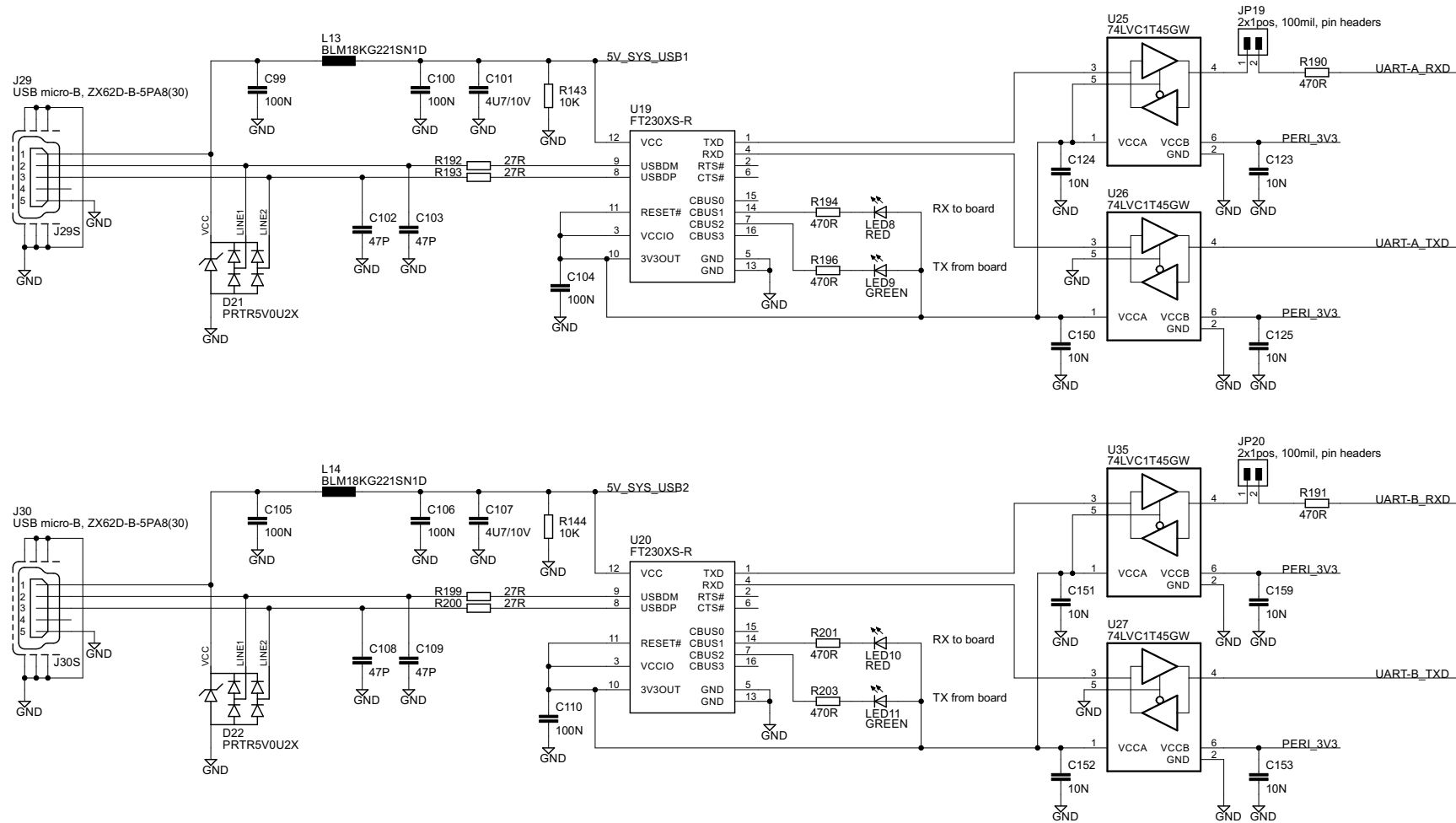
TITLE: uCOM Carrier board rev B

Document Number:

Date: not saved!

Sheet: 14/25

UART-to-USB bridge interfaces



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TITLE: uCOM Carrier board rev B

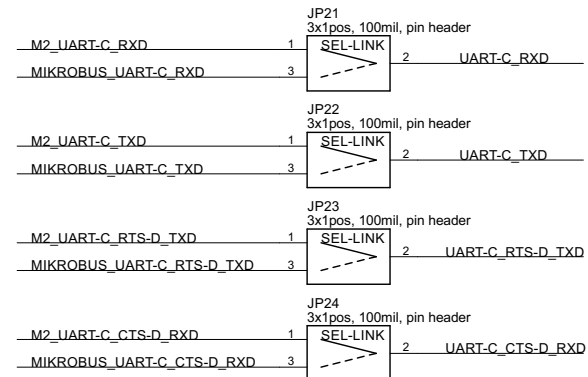
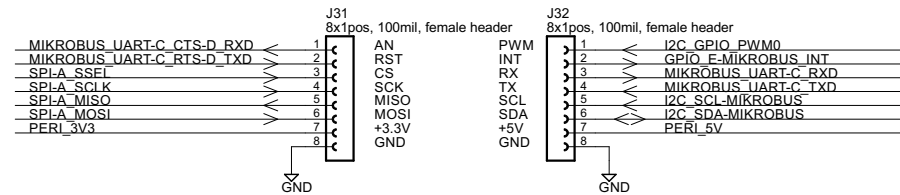
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Date: not saved!

Sheet: 15/25

Mikrobus/Click Module Interface

Mikrobus/Click Module Interface



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TITLE: uCOM Carrier board rev B

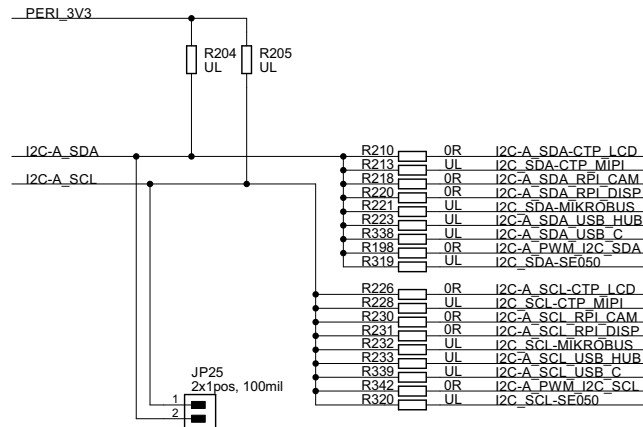
Document Number:

Date: not saved!

Sheet: 16/25

I2C Connections

I2C-A

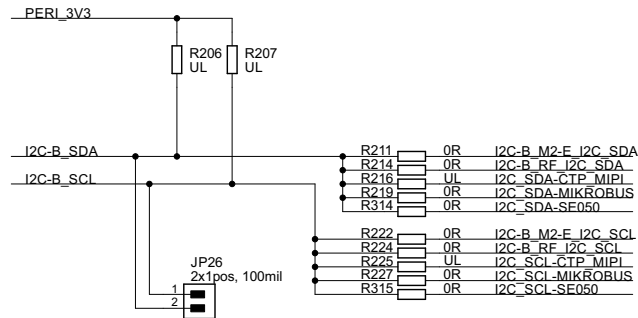


64kbit E2PROM on uCOM: 24LC64
8-bit I2C address (0xAA/0xAB): 1.0.1.0.1.1.RW
7-bit I2C address (0x55): 1.0.1.0.1.1

Optional 1Kbit I2C-E2PROM with EUI-48: 24AA025E48T
8-bit I2C address (0xA6/0xA7): 1.0.1.0.1.1.RW
7-bit I2C address (0x53): 1.0.1.0.1.1

GPIO expander: PCA9530
8-bit I2C address (0xC2/0xC3): 1.1.0.0.0.0.ADDR.RW
7-bit I2C address (0x61): 1.1.0.0.0.0.ADDR

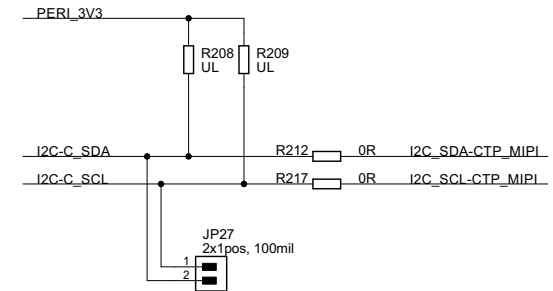
I2C-B



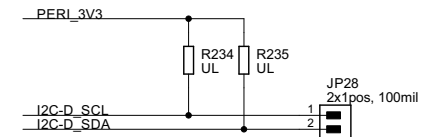
GPIO expander: PCA6416A
8-bit I2C address (0x42/0x43): 0.1.0.0.0.0.ADDR.RW
7-bit I2C address (0x21): 0.1.0.0.0.0.ADDR

GPIO expander: PCA6408A on M.2
8-bit I2C address (0x40/0x41): 0.1.0.0.0.0.RW
7-bit I2C address (0x20): 0.1.0.0.0.0

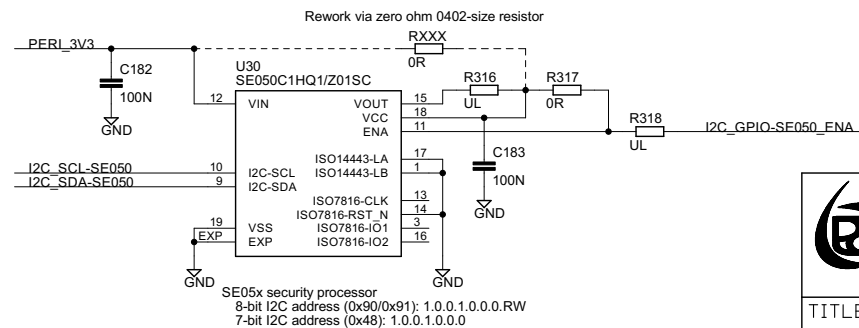
I2C-C



I2C-D



NXP SE050 security processor



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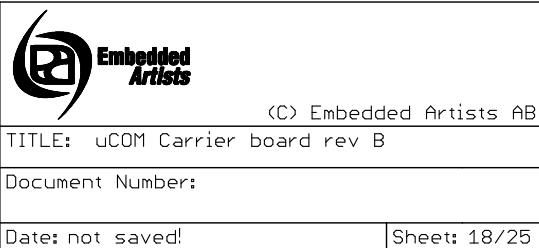
TITLE: uCOM Carrier board rev B

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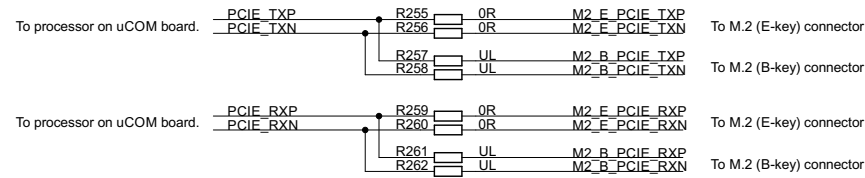
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Sheet: 17/25

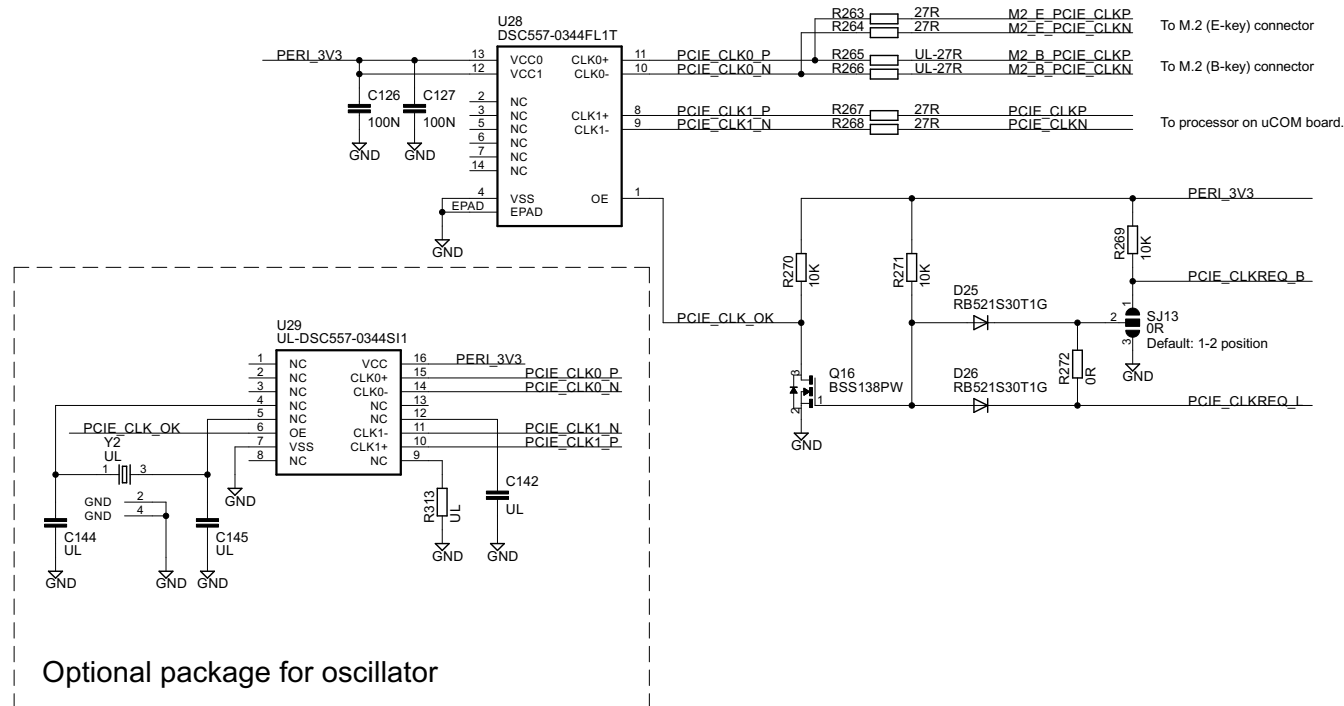
M.2 (NGFF) Key E Connector



PCIe Signal Routing



100MHz clock generator



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TITLE: uCOM Carrier board rev B

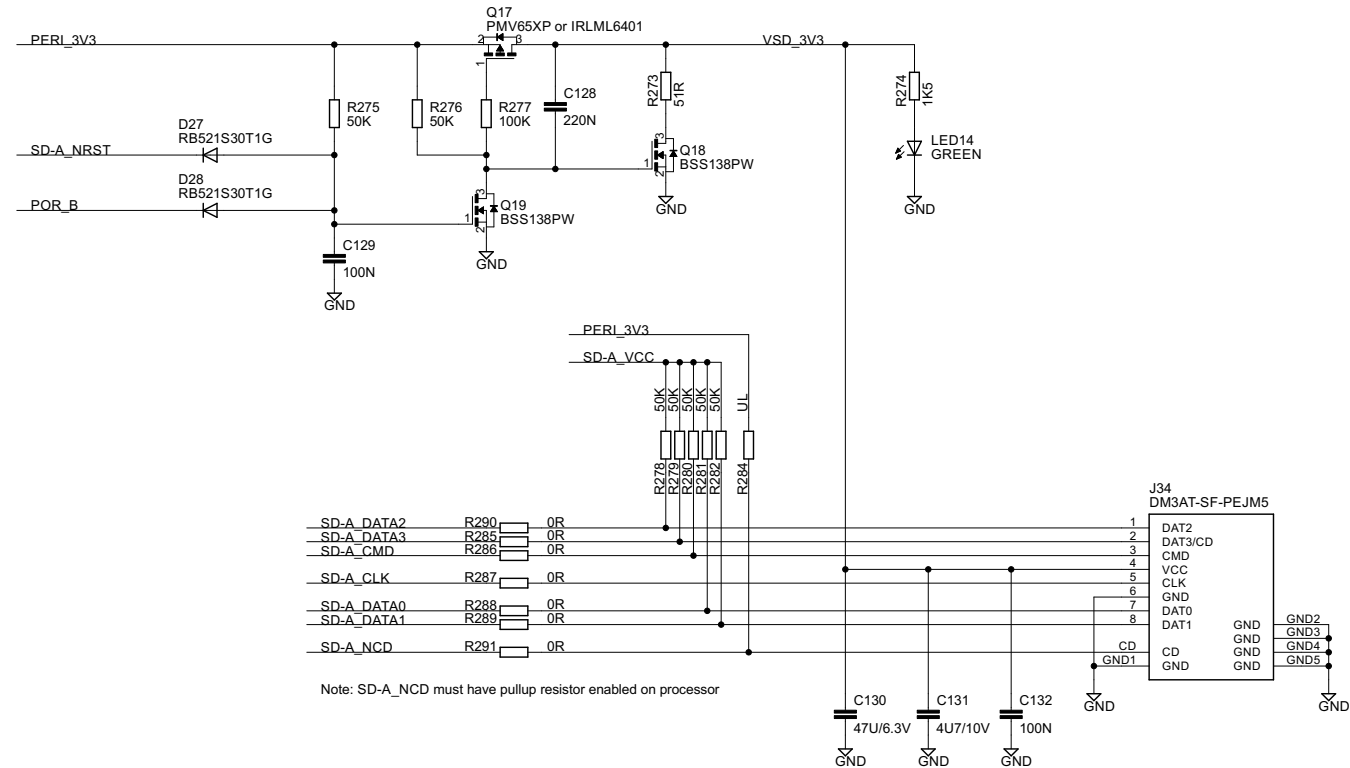
Document Number:

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Sheet: 19/25

uSD card interface

Power Switch for SD3.0



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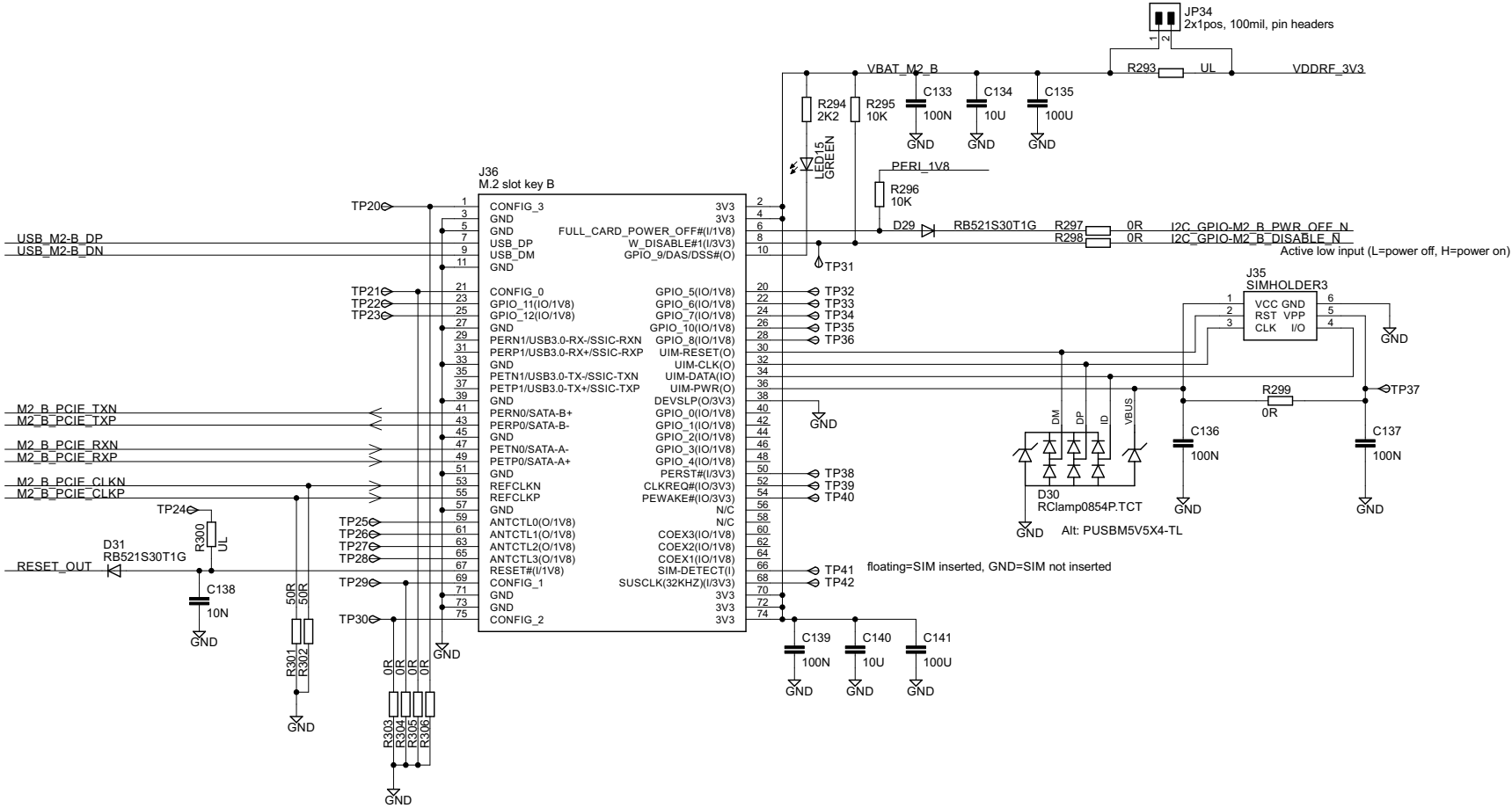
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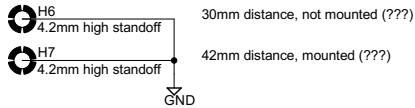
Date: not saved!

Sheet: 20/25

M.2 (NGFF) Key B Connector (USB Host and PCIe Interfaces)



Standoffs for M.2 connector, placed at 30mm and 42mm distance from connector



(C) Embedded Artists AB

TITLE: uCOM Carrier board rev B

Document Number:

Date: not saved!

Sheet: 21/25

100/10Mbps Ethernet-PHY Adapter for RT1064 uCOM

Separate adapter board

Connector "D"
(in silkscreen on PCB)
(for RT1064)

0.5mm pitch, top and bottom contacts
XF2W-4015-1A or 68714014022

VLED- J17-1
VLED+ J17-2
GND J17-3
VDD J17-4

ENET_3V3 J17-5
ENET_TX_CLK J17-6
ENET_RXER J17-7
ENET_RXD0 J17-8
ENET_RXD1 J17-9
ENET_CRS_DV J17-10
ENET_PHYAD0 J17-11
ENET_PHYAD1 J17-12
ENET_PHYAD2 J17-13

ENET_TXD0 J17-14
ENET_TXD1 J17-15
ENET_TXEN J17-16
ENET_TXD0 J17-17
ENET_TXD1 J17-18
ENET_TXEN J17-19
ENET_TXD0 J17-20
ENET_TXD1 J17-21
ENET_TXEN J17-22

ENET_TXD0 J17-23
ENET_TXD1 J17-24
ENET_TXEN J17-25
ENET_TXD0 J17-26
ENET_TXD1 J17-27
ENET_TXEN J17-28
ENET_TXD0 J17-29
ENET_TXD1 J17-30
ENET_TXEN J17-31

ENET_TXD0 J17-32
ENET_TXD1 J17-33
ENET_TXEN J17-34
ENET_TXD0 J17-35
ENET_TXD1 J17-36
ENET_TXEN J17-37
ENET_TXD0 J17-38
ENET_TXD1 J17-39
ENET_TXEN J17-40

ENET_TXD0 J17-41
ENET_TXD1 J17-42
ENET_TXEN J17-43
ENET_TXD0 J17-44
ENET_TXD1 J17-45
ENET_TXEN J17-46
ENET_TXD0 J17-47
ENET_TXD1 J17-48
ENET_TXEN J17-49

ENET_TXD0 J17-50
ENET_TXD1 J17-51
ENET_TXEN J17-52
ENET_TXD0 J17-53
ENET_TXD1 J17-54
ENET_TXEN J17-55
ENET_TXD0 J17-56
ENET_TXD1 J17-57
ENET_TXEN J17-58

ENET_TXD0 J17-59
ENET_TXD1 J17-60
ENET_TXEN J17-61
ENET_TXD0 J17-62
ENET_TXD1 J17-63
ENET_TXEN J17-64
ENET_TXD0 J17-65
ENET_TXD1 J17-66
ENET_TXEN J17-67

ENET_TXD0 J17-68
ENET_TXD1 J17-69
ENET_TXEN J17-70
ENET_TXD0 J17-71
ENET_TXD1 J17-72
ENET_TXEN J17-73
ENET_TXD0 J17-74
ENET_TXD1 J17-75
ENET_TXEN J17-76

ENET_TXD0 J17-77
ENET_TXD1 J17-78
ENET_TXEN J17-79
ENET_TXD0 J17-80
ENET_TXD1 J17-81
ENET_TXEN J17-82
ENET_TXD0 J17-83
ENET_TXD1 J17-84
ENET_TXEN J17-85

ENET_TXD0 J17-86
ENET_TXD1 J17-87
ENET_TXEN J17-88
ENET_TXD0 J17-89
ENET_TXD1 J17-90
ENET_TXEN J17-91
ENET_TXD0 J17-92
ENET_TXD1 J17-93
ENET_TXEN J17-94

ENET_TXD0 J17-95
ENET_TXD1 J17-96
ENET_TXEN J17-97
ENET_TXD0 J17-98
ENET_TXD1 J17-99
ENET_TXEN J17-100
ENET_TXD0 J17-101
ENET_TXD1 J17-102
ENET_TXEN J17-103

PHY ADDR: 00-010 (2)
Address = 00-xxx

Interface mode: RMII
001 = RMII
101 = RMII Back-to-Back

Isolate more: enabled
Pull-up = Enable
Pull-down (default) = Disable

Nway Auto-Negotiation
Pull-up (default) = Enable
Pull-down = Disable

Speed mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps

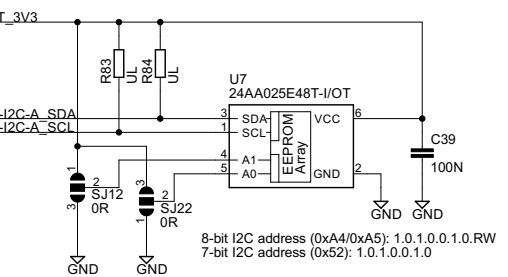
DUPLEX mode
Pull-up (default) = Half Duplex
Pull-down = Full Duplex

Interface mode: RMII
Pull-up = PHY Address 0 set as unique PHY addr
Pull-down (default) = PHY Address 0 set as broadcast PHY addr

NAND Tree Mode
Pull-up (default) = Disable
Pull-down = Enable

RJ45 Connector with
integrated magnetics

1Kbit I2C-E2PROM with EUI-48



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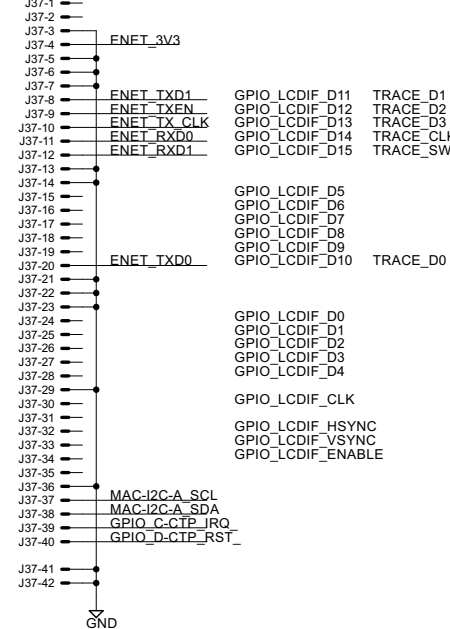
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100/10Mbps Ethernet-PHY Adapter for RT1176 uCOM

Separate adapter board (from previous schematic page)

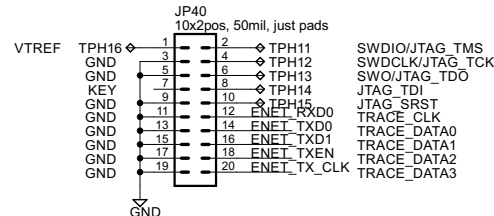
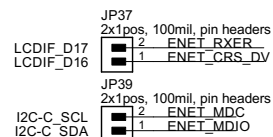
Connector "D"
(in silkscreen on PCB)
(for RT1176)

0.5mm pitch, top and bottom contacts
XF2W-4015-1A or 68714014022



iMX8M Mini	RT1064	RT1176
	Connect to J17 to get second Ethernet I/F	Connect to J37 to get second Ethernet interface
JA pin 33 (GPIO_LCDIF_CLK) JA pin 35 (GPIO_LCDIF_HSYNC) JA pin 37 (GPIO_LCDIF_VSYNC) JA pin 39 (GPIO_LCDIF_ENABLE)	MDC	
SAI1_TXD0 BT_CFG8-0	MDIO	
JA pin 43 (GPIO_LCDIF_D0) JA pin 45 (GPIO_LCDIF_D1) JA pin 47 (GPIO_LCDIF_D2) JA pin 49 (GPIO_LCDIF_D3)	SAI1_TXD1 BT_CFG9-0 SAI1_TXD2 BT_CFG10-0 SAI1_TXD3 BT_CFG11-1 SAI1_TXD4 BT_CFG12-0	BT_CFG10 BT_CFG11 BT_CFG12 BT_CFG13
JA pin 53 (GPIO_LCDIF_D4) JA pin 55 (GPIO_LCDIF_D5) JA pin 57 (GPIO_LCDIF_D6) JA pin 59 (GPIO_LCDIF_D7)	SAI1_TXD5 BT_CFG13-1 SAI1_TXD6 BT_CFG14-0 SAI1_TXD7 BT_CFG15-0	BT_CFG14 BT_CFG15 BT_CFG16 BT_CFG17
JA pin 63 (GPIO_LCDIF_D8) JA pin 65 (GPIO_LCDIF_D9) JA pin 67 (GPIO_LCDIF_D10) JA pin 69 (GPIO_LCDIF_D11)	SAI1_RXD0 BT_CFG0-0 SAI1_RXD1 BT_CFG1-1 SAI1_RXD2 BT_CFG2-1	BT_CFG6 BT_CFG7 BT_CFG8 BT_CFG9
JA pin 73 (GPIO_LCDIF_D12) JA pin 75 (GPIO_LCDIF_D13) JA pin 77 (GPIO_LCDIF_D14) JA pin 79 (GPIO_LCDIF_D15)	SAI1_RXD3 BT_CFG3-0 SAI1_RXD4 BT_CFG4-0 SAI1_RXD5 BT_CFG5-1 SAI1_RXD6 BT_CFG6-1	BT_CFG10 BT_CFG11
JA pin 83 (GPIO_LCDIF_D16) JA pin 85 (GPIO_LCDIF_D17)	SAI1_RXD7 BT_CFG7-0	RX_EN RX_ER

Support for accessing iMX RT1176 Trace Signals



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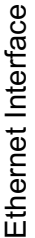
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Sheet: 24/25

1000/100/10Mbps Ethernet-PHY Adapter for i.MX93

0.5mm pitch, top and bottom contacts
XF2W-4015-1A or 68714014022



GPIO-CSI_RST-DATA	1	—
GPIO-CSI_PWR-CLK	2	—
GPIO_JA84	3	—

```
PHYAD[210]: 001
PLLOFF: 0
TXDLY: 0
RXDLY: 1
CFG_EXT: 0 (internal powering of IO pads)
CFG_LDO[10]: 10 for 1.8V
```



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