iMX8M COM Board Datasheet

Get Up-and-Running Quickly and
Start Developing Your Application On Day 1!

Embedded Artists

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1 Document Revision History

Revision	*Date*	*Description*
PA1	2019-08-14	First version.

2 Introduction

This document is a datasheet that specifies and describes the *iMX8M COM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX8M COM Board* is a Computer-on-Module (COM) based on NXP's quad/dual-core ARM Cortex-A53 / M4 i.MX 8M System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM quad/dual-core Cortex-A53 / M4 based design. The Cortex-A53 cores runs at up to 1.5GHz and the Cortex-M4 core at up to 266 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A53 cores and a Real-Time OS (RTOS) on the Cortex-M4. This architecture is ideal for real time applications where Linux cannot be used for all time critical task. The Cortex-M4 can handle (real time) critical tasks and can also be used to lower the power consumption.

The *iMX8M COM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR4 memory sub-system reduce the power consumption.

The SoC is part of the scalable i.MX 6/7/8 product family. There is a range of i.MX 6/7/8 COM Boards from Embedded Artists with single, dual and quad Cortex-A cores, with or without a heterogeneous Cortex-M core. All boards share the same basic pinning for maximum flexibility and performance scalability.

The *iMX8M COM Board* has a very small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX8M COM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX8M COM Board*.

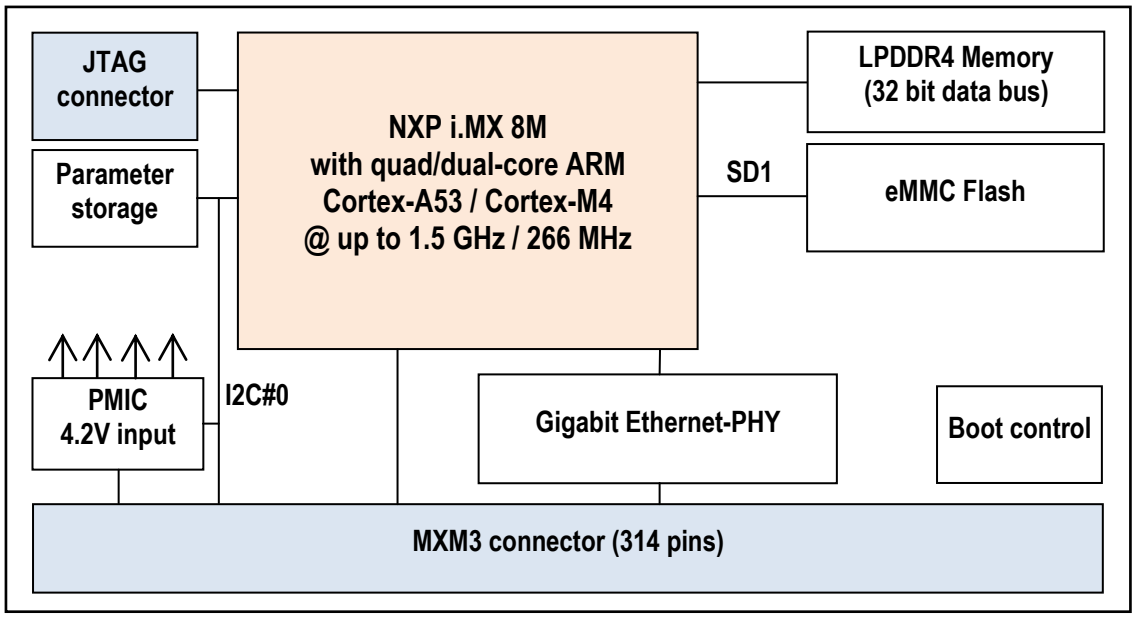


Figure 1 – iMX8M COM Board Block Diagram

The *iMX8M COM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX6/7/8 COM Boards* from Embedded Artists and the general, so called, EACOM specification is found in separate document.

2.2 Software

The *iMX8M COM Board* has Board Support Packages (BSPs) for Embedded Linux and Android. Precompiled images are available. Embedded Artists works with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX8M COM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 8M is a powerful SoC. The full specification can be found in NXP's *i.MX 8M Datasheet* and *i.MX 8M Reference Manual*. The table below lists the main features and functions of the *iMX8M COM board* - which represents Embedded Artists integration of the i.MX 8M SoC. Due to pin configuration some functions and interfaces of the i.MX 8M many not be available at the same time. See i.MX 8M SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature		iMX8M COM Board
CPUs	NXP SoC	Quad commercial temp. range Dual commercial temp. range Quad industrial temp. range Dual industrial temp. range	MIMX8MQ6DVAJZA (0 - 70° C) MIMX8MD7DVAJZA (0 - 70° C) MIMX8MQ6CVAHZA (-40 - 85° C) MIMX8MD6CVAHZA (-40 - 85° C)
	CPU Cores		4/2x Cortex-A53 1x Cortex-M4F with MPU/FPU
	L1 Instruction cache		32 KByte for each Cortex-A53

		16 KByte on Cortex-M4
	L1 Data cache	32 KByte for each Cortex-A53 16 KByte on Cortex-M4
	L2 Cache on Cortex-A53 cores	1 MByte
	TCM on Cortex-M4	256 KByte
	NEON SIMD media accelerator on Cortex-A53	✓
	Maximum CPU frequency	1.3/1.5 MHz on Cortex-A53 266 MHz on Cortex-M4
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage	✓
	System JTAG controller	✓
	Resource Domain Controller (RDC)	✓
Memory	LPDDR4 RAM Size	1 GByte, default. Other on request.
	LPDDR4 RAM Speed	3200 MT/s
	LPDDR4 RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	8 GByte, default. Other on request.
Graphical Processing	Multimedia Graphics Processing Unit (GPU)	4 Shader, OpenGL/ES 3.1, Vulkan, OpenCL 1.2
	Video Processing Unit (VPU)	4Kp60 HEVC/H.265, H.264, VP9 Decoder
	Video Processing Unit (VPU)	1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 Decoder
Graphical Output	HDMI 2.0a Tx	✓
	MIPI-DSI, 4 lanes	✓
Graphical Input	2x MIPI-CSI, 4 lanes	✓
Audio I/O	Multi-channel Audio Interfaces	6x I2S/SAI with TDM support (20+ channels, each 32 bits@384KHz)
	SPDIF TX and RX	✓
	DSD512	✓
	HDMI Audio Return Channel (ARC)	✓
Connectivity Interfaces (all functions are not available at	1000/100/10 Mbps Gigabit Ethernet controller with support for EEE, Audio Video Bridging (AVB) and IEEE1588.	✓ with on-board PHY
	QuadSPI with support for XIP	✓

the same time)	2x PCIe Gen2 (1 lane)	✓
	2x USB3.0/2.0 OTG ports with Type C support	✓
	1x SD3.0/MMC 5.0	✓ SD1 interface used on-board to eMMC
	3x SPI, 4x UART, 4x I²C	✓
	4x PWM, GPIOs, WDOG	✓
Other	PMIC (BD71837MWV) supporting DVFS techniques for low power modes	✓
	E2PROM storing board information and Ethernet MAC address	✓
	On-board RTC via PMIC (BD71837MWV)	✓
	On-board watchdog functionality	✓

2.4 Interface Overview

The table below lists the interfaces that are specified in the EACOM specification (see separate document for details) and what is supported by the *iMX8M COM board*.

Interface	EACOM specification	iMX8M COM Board	Note
UART	3 ports (two 4 wire and one 2 wire)	3 ports	More ports available as alternative pin functions
SPI	2 ports	2 port	More ports available as alternative pin functions
I2C	3 ports	2 ports	I2C-C is dedicated to HDMI DDC The third and fourth I2C ports are available on alternative pins
SD/MMC	2 ports (one 4 databits and one 8 databits)	1 port	4 databits
Parallel LCD	24 databits and CLK/HS/VS/DE	-	Not supported
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	-	Not supported
LVDS LCD	2 ports (18/24 bit LVDS data)	-	Optional support with MIPI-DSI to LVDS bridge
HDMI (TDMS)		1 port	
Parallel Camera		-	Not supported
Serial Camera	CSI, 4 lane	1 port, 4 lanes	An additional 4 lane interface is available on alternative pins

Gigabit Ethernet	2 ports	1 port	Gigabit speed supported
PCIe	1 post, 1 lane	1 port, 1 lane	An additional PCIe interface is available on alternative pins
SATA	1 port	-	Not supported
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	2x USB3.0/2.0 OTG ports	ID-pin on second USB3.0 port is available on alternative/non-standard pin
SPDIF	1 TX/RX port	1 port	
CAN	2 ports	-	Not supported
I2S/SSI/AC97	1 port (4 wire synchronous plus MCLK)	1 port	More ports available as alternative pin functions.
Analog audio	Stereo output	-	Not supported
GPIO	9 pins	7 pins	More GPIO pins are available as alternative pin functions.
PWM	1 pin	1 pin	More pins are available as alternative pin functions.
ADC	8 inputs	-	Not supported
Type specific	39 pins	39 pins, incl MIPI-DSI port	All type specific pins connected to i.MX 8M pins.
Power	10 VIN, VBAT and 45 GND	10 VIN, VBAT and 45 GND	About 15% of the pins are ground pins. Four grounded mounting holes are also present.

2.5 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX8M COM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX8MDQLQCEC, i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products, latest revision
- IMX8MDQLQIEC, i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Industrial Products, latest revision

- IMX8MDQLQRM, i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors Reference Manual, latest revision
- IMX8MDQLQSRM, Security Reference Manual for i.MX 8M Dual/8M QuadLite/8M Quad, latest revision
- IMX8MDQLQ, Chip Errata for the i.MX 8M, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12118, i.MX 8M Quad Power Consumption Measurement, latest revision
- AN12147, i.MX 8M Dual / 8M QuadLite / 8M Quad Product Lifetime Usage, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has created the *EACOM Board Specification* that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the EACOM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the EACOM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

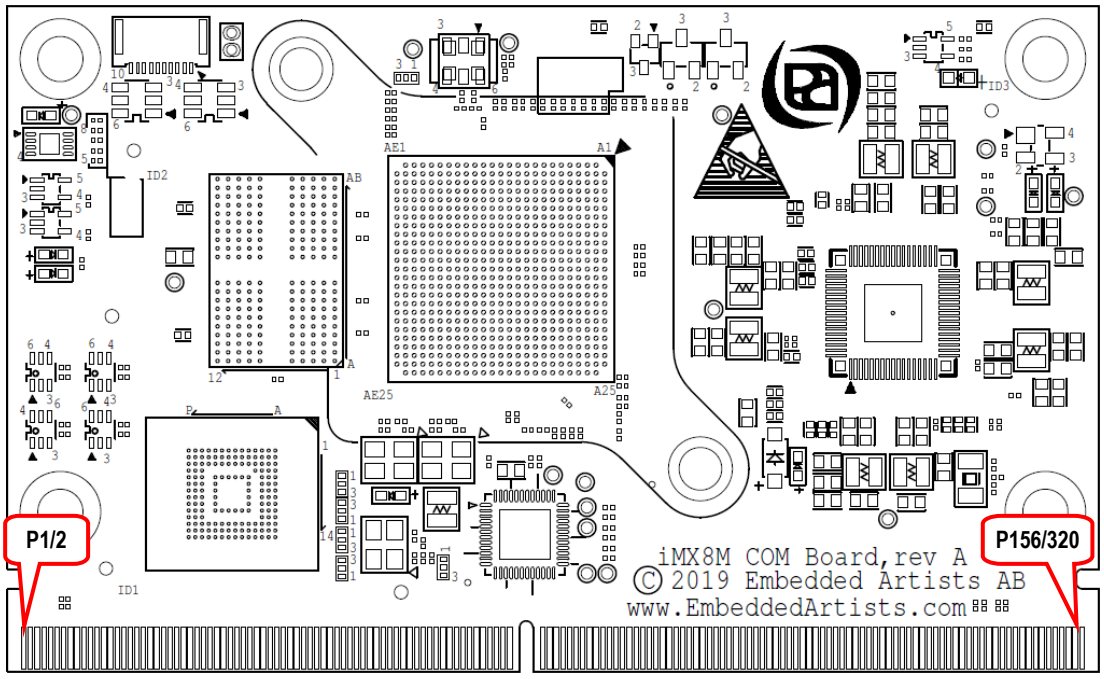


Figure 2 – EACOM Board Pin Numbering, Top Side

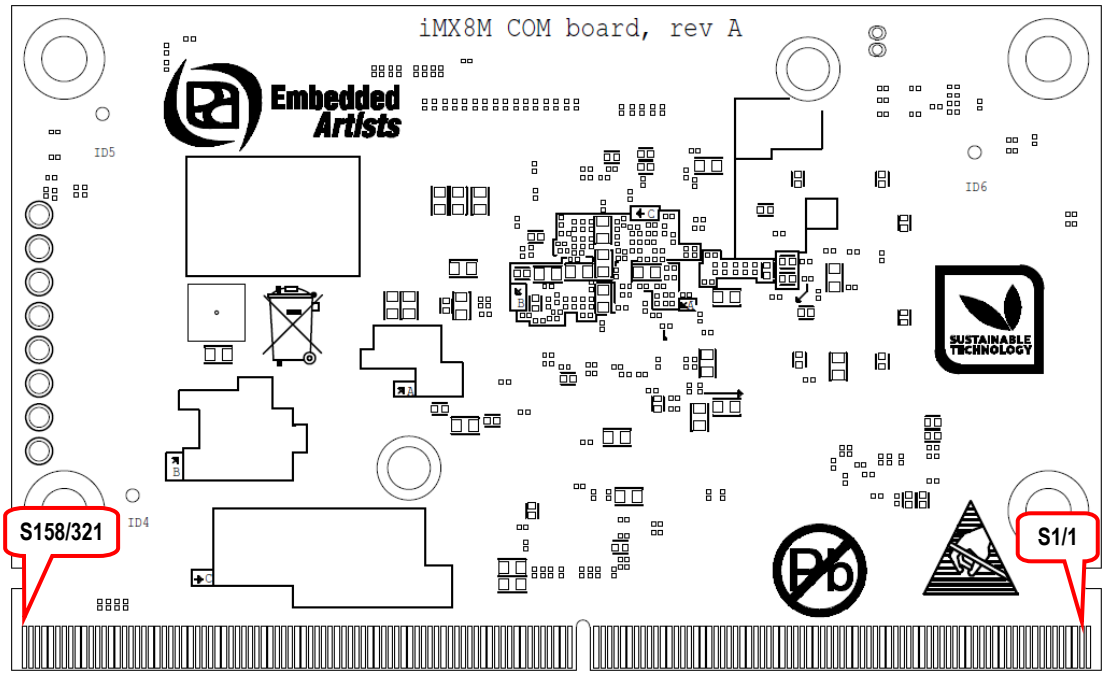


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different EACOM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 8M Ball Name	The name of the ball of the i.MX 8M SoC (or other component on the EACOM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 45 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	i.MX 8M Ball Name	Alternative pin functions?	Notes
P1/2	GPIO-F	SD2_WP	Yes	Controlled by alternative pin function GPIO2_IO20. **Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra high speed SD memory card.
P2/4	GPIO-E	I2C4_SCL	Yes	Controlled by alternative pin function GPIO5_IO20
P3/6	GPIO-D	SD2_CD_B	Yes	Controlled by alternative pin function GPIO2_IO12.

				Note: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra high speed SD memory card.
P4/8	GPIO-C	SD2_RESET_B	Yes	Controlled by alternative pin function GPIO2_IO19. **Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra high speed SD memory card.
P5/10	SD_D1	SD1_D1	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P6/12	SD_D0	SD1_D0	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P7/14	SD_CLK	SD1_CLK	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P8/16	SD_CMD	SD1_CMD	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P9/18	SD_D3	SD1_D3	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P10/20	SD_D2	SD1_D2	Yes	**Note**: Logic level (3.3V or 1,8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P11/22	SD_VCC	NVCC_SD2		Supply voltage for SD interface (1.85V or 3.2V). This is an output but should never be used to anything else than the SD interface.
P12/24	MMC_D1			
P13/26	MMC_D0			
P14/28	MMC_D7			
P15/30	MMC_D6			
P16/32	MMC_CLK			
P17/34	MMC_D5			
P18/36	MMC_CMD			
P19/38	MMC_D4			
P20/40	MMC_D3			
P21/42	MMC_D2			
P22/44	GND			
P23/46	HDMI_TXC_N	HDMI_CLKN		
P24/48	HDMI_TXC_P	HDMI_CLKP		
P25/50	GND			
P26/52	HDMI_TXD0_N	HDMI_TXN0		
P27/54	HDMI_TXD0_P	HDMI_TXP0		
P28/56	HDMI_HPD	HDMI_HPD		
P29/58	HDMI_TXD1_N	HDMI_TXN1		
P30/60	HDMI_TXD1_P	HDMI_TXP1		
P31/62	GND			
P32/64	HDMI_TXD2_N	HDMI_TXN2		
P33/66	HDMI_TXD2_P	HDMI_TXP2		
P34/68	HDMI_CEC	HDMI_CEC		
P35/70	GND			
P36/72	ETH1_MD1_P	ETH_TRXP1		Connects to Ethernet-PHY AR8031, pin 14
P37/74	ETH1_MD1_N	ETH_TRXN1		Connects to Ethernet-PHY AR8031, pin 15

P38/76	GND			
P39/78	ETH1_MD0_P	ETH_TRXP0		Connects to Ethernet-PHY AR8031, pin 11
P40/80	ETH1_MD0_N	ETH_TRXN0		Connects to Ethernet-PHY AR8031, pin 12
P41/82	ETH1_LINK1000	ETH_LED1000		Connects to Ethernet-PHY AR8031, pin 24
P42/84	ETH1_ACT	ETH_LEDACT		Connects to Ethernet-PHY AR8031, pin 23
P43/86	ETH1_LINK	ETH_LED10_100		Connects to Ethernet-PHY AR8031, pin 26
P44/88	ETH1_MD3_N	ETH_TRXN3		Connects to Ethernet-PHY AR8031, pin 21
P45/90	ETH1_MD3_P	ETH_TRXP3		Connects to Ethernet-PHY AR8031, pin 20
P46/92	GND			
P47/94	ETH1_MD2_N	ETH_TRXN2		Connects to Ethernet-PHY AR8031, pin 18
P48/96	ETH1_MD2_P	ETH_TRXP2		Connects to Ethernet-PHY AR8031, pin 17
P49/98	GND			
P50/100	ETH2_MD1_P			
P51/102	ETH2_MD1_N			
P52/104	GND			
P53/106	ETH2_MD0_P			
P54/108	ETH2_MD0_N			
P55/110	ETH2_LINK1000			
P56/112	ETH2_ACT			
P57/114	ETH2_LINK			
P58/116	ETH2_MD3_N			
P59/118	ETH2_MD3_P			
P60/120	GND			
P61/122	ETH2_MD2_N			
P62/124	ETH2_MD2_P			
P63/126	GND			
P64/128	USB_O1_DN	USB1_DN	No	
P65/130	USB_O1_DP	USB1_DP	No	
P66/132	USB_O1_OTG_ID	USB1_ID	No	
P67/134	USB_O1_SSTXN	USB1_TXN	No	
P68/136	USB_O1_SSTXP	USB1_TXP	No	
P69/138	GND			
P70/140	USB_O1_SSRXN	USB1_RXN	No	
P71/142	USB_O1_SSRXP	USB1_RXP	No	
P72/144	USB_O1_VBUS	USB1_VBUS	No	
P73/146	USB_O1_PWR_EN	GPIO12	Yes	Controlled by alternative pin function USB1_PWR
P74/148	USB_O1_OC	GPIO13	Yes	Controlled by alternative pin function USB1_OC
150	Non existing pin			
152	Non existing pin			
154	Non existing pin			
156	Non existing pin			
P75/158	USB_H1_PWR_EN	GPIO14	Yes	Controlled by alternative pin function USB2_PWR

P76/160	USB_H1_OC	GPIO15	Yes	Controlled by alternative pin function USB2_OC
P77/162	GND			
P78/164	USB_H1_DN	USB2_DN	No	
P79/166	USB_H1_DP	USB2_DP	No	
P80/168	USB_H1_SSTXN	USB2_TXN	No	
P81/170	USB_H1_SSTXP	USB2_TXP	No	
P82/172	GND			
P83/174	USB_H1_SSRXN	USB2_RXN	No	
P84/176	USB_H1_SSRXP	USB2_RXP	No	
P85/178	USB_H1_VBUS	USB2_VBUS	No	
P86/180	USB_H2_PWR_EN	USB2_ID	No	Non-standard pin allocation (USB Host port #2 on i.MX 8M does not exist).
P87/182	USB_H2_OC	ONOFF	No	Non-standard pin allocation (USB Host port #2 on i.MX 8M does not exist).
P88/184	GND			
P89/186	USB_H2_DN			
P90/188	USB_H2_DP			
P91/190	GND			
P92/192	COM board specific	GPIO11	(No)	Allocated for on-board Ethernet-Phy interrupt signal
P93/194	COM board specific	GPIO10	(No)	Allocated for on-board Ethernet-Phy Wake-on-LAN signal
P94/196	COM board specific	GPIO9	(No)	Allocated for on-board Ethernet-Phy reset signal
P95/198	COM board specific	GPIO3	(No)	Allocated for on-board PMIC interrupt signal
P96/200	COM board specific	GPIO2	(No)	Allocated for on-board watchdog signal
P97/202	COM board specific	NAND_RE_B	Yes	Controlled by alternative pin function GPIO3_IO15
P98/204	COM board specific	NAND_DATA7	Yes	Controlled by alternative pin function GPIO3_IO13
P99/206	COM board specific	NAND_DATA 6	Yes	Controlled by alternative pin function GPIO3_IO12
P100/208	COM board specific	NAND_DATA 5	Yes	Controlled by alternative pin function GPIO3_IO11
P101/210	COM board specific	NAND_DATA 4	Yes	Controlled by alternative pin function GPIO3_IO10
P102/212	COM board specific	NAND_CE3_B	Yes	Controlled by alternative pin function GPIO3_IO4
P103/214	COM board specific	NAND_CE2_B	Yes	Controlled by alternative pin function GPIO3_IO3
P104/216	COM board specific	NAND_CLE	Yes	Controlled by alternative pin function GPIO3_IO5
P105/218	COM board specific	NAND_DQS	Yes	Controlled by alternative pin function GPIO3_IO14
P106/220	COM board specific	NAND_DATA3	Yes	Controlled by alternative pin function GPIO3_IO9
P107/222	COM board specific	NAND_DATA2	Yes	Controlled by alternative pin function GPIO3_IO8
P108/224	COM board specific	NAND_DATA1	Yes	Controlled by alternative pin function GPIO3_IO7
P109/226	COM board specific	NAND_DATA0	Yes	Controlled by alternative pin function GPIO3_IO6
P110/228	COM board specific	NAND_CE1_B	Yes	Controlled by alternative pin function GPIO3_IO2
P111/230	COM board specific	NAND_CE0_B	Yes	Controlled by alternative pin function GPIO3_IO1
P112/232	COM board specific	NAND_ALE	Yes	Controlled by alternative pin function GPIO3_IO0
P113/234	COM board specific	NAND_READY_B	Yes	Controlled by alternative pin function GPIO3_IO16
P114/236	COM board specific	NAND_WE_B	Yes	Controlled by alternative pin function GPIO3_IO17
P115/238	COM board specific	NAND_WP_N	Yes	Controlled by alternative pin function GPIO3_IO18
P116/240	COM board specific	GPIO1	Yes	Controlled by alternative pin function GPIO1_IO1

P117/242	COM board specific	GPIO0	Yes	Controlled by alternative pin function GPIO1_IO0
P118/244	GND			
P119/246	SPI-B_SSEL	ECSPI2_SS0	Yes	Controlled by alternative pin function ECSPI2_SS0
P120/248	SPI-B_MOSI	ECSPI2_MOSI	Yes	Controlled by alternative pin function ECSPI2_MOSI
P121/250	SPI-B_MISO	ECSPI2_MISO	Yes	Controlled by alternative pin function ECSPI2_MISO
P122/252	SPI-B_CLK	ECSPI2_SCLK	Yes	Controlled by alternative pin function ECSPI2_SCLK
P123/254	SPI-A_SSEL	ECSPI1_SS0	Yes	Controlled by alternative pin function ECSPI1_SS0
P124/256	SPI-A_MOSI	ECSPI1_MOSI	Yes	Controlled by alternative pin function ECSPI1_MOSI
P125/258	SPI-A_MISO	ECSPI1_MISO	Yes	Controlled by alternative pin function ECSPI1_MISO
P126/260	SPI-A_CLK	ECSPI1_SCLK	Yes	Controlled by alternative pin function ECSPI1_SCLK
P127/262	GND			
P128/264	UART-C_RXD	UART3_RXD	Yes	Controlled by alternative pin function UART3_RXD
P129/266	UART-C_TXD	UART3_TXD	Yes	Controlled by alternative pin function UART3_TXD
P130/268	UART-B_RXD	UART2_RXD	Yes	Controlled by alternative pin function UART2_RXD
P131/270	UART-B_CTS	UART4_RXD	Yes	Controlled by alternative pin function UART2_CTS_B
P132/272	UART-B_RTS	UART4_TXD	Yes	Controlled by alternative pin function UART2_RTS_B
P133/274	UART-B_TXD	UART2_TXD	Yes	Controlled by alternative pin function UART2_TXD
P134/276	UART-A_RXD	UART1_TXD	Yes	Controlled by alternative pin function UART1_RXD
P135/278	UART-A_CTS	GPIO8	Yes	Controlled by alternative pin function UART1_CTS_B
P136/280	UART-A_RTS	GPIO5	Yes	Controlled by alternative pin function UART1_RTS_B
P137/282	UART.A_TXD	UART1_TXD	Yes	Controlled by alternative pin function UART1_TXD
P138/284	PWM	SPDIF_EXT_CLK	Yes	Controlled by alternative pin function PWM1_OUT
P139/286	GPIO-B	GPIO7	Yes	GPIO2 controlled by alternative pin function GPIO1_IO7
P140/288	GPIO-A	GPIO6	Yes	GPIO1 controlled by alternative pin function GPIO1_IO6
P141/290	PERI_PWR_EN			Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*. This signal is a copy of the on-board generated 3.3V supply.
P142/292	RESET_IN			Reset input, active low. Pull signal low to activate reset. There is no need to pull signal high externally.
P143/294	RESET_OUT			Reset (open drain) output, active low. Driven low during reset. Has a 10Kohm pull-up resistor to on-board generated 3.3V supply.
P144/296	VIN_SELECT			This output is connected to VIN via a 1Kohm resistor to signal that supply voltage VIN shall be 4.2V. This is for carrier boards that can support EACOM boards that require 3.3V on VIN (in this case, this pin is connected to ground).
P145/298	VBAT_RTC			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	ISP_ENABLE			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM and place the i.MX 8M SoC in USB OTG boot mode after a power cycle).
P147/302	VIN			Main input voltage supply (4.2V)
P148/304	VIN			Main input voltage supply (4.2V)
P149/306	VIN			Main input voltage supply (4.2V)
P150/308	VIN			Main input voltage supply (4.2V)
P151/310	VIN			Main input voltage supply (4.2V)

P152/312	VIN	Main input voltage supply (4.2V)
P153/314	VIN	Main input voltage supply (4.2V)
P154/316	VIN	Main input voltage supply (4.2V)
P155/318	VIN	Main input voltage supply (4.2V)
P156/320	VIN	Main input voltage supply (4.2V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	i.MX 8M Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	SAI2_RXFS	Yes	Controlled by alternative pin function GPIO4_IO21
S2/3	MQS_LEFT	SAI2_RXC	Yes	Controlled by alternative pin function GPIO4_IO22
S3/5	GND			
S4/7	AUDIO_TXFS	SAI2_TXFS	Yes	Controlled by alternative pin function SAI2_TXFS
S5/9	AUDIO_RXD	SAI2_RXD	Yes	Controlled by alternative pin function SAI2_RXD
S6/11	AUDIO_TXC	SAI2_TXC	Yes	Controlled by alternative pin function SAI2_TXC
S7/13	AUDIO_TXD	SAI2_TXD	Yes	Controlled by alternative pin function SAI2_TXD
S8/15	AUDIO_MCLK	SAI2_MCLK	Yes	Controlled by alternative pin function SAI2_MCLK
S9/17	GND			
S10/19	SPDIF_IN	SPDIF_RX	Yes	Controlled by alternative pin function SPDIF_RX
S11/21	SPDIF_OUT	SPDIF_TX	Yes	Controlled by alternative pin function SPDIF_TX
S12/23	CAN2_TX			
S13/25	CAN2_RX			
S14/27	CAN1_TX			
S15/29	CAN1_RX			
S16/31	GND			
S17/33	LVDS1_D3_P	MIPI_CSI2_D3P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S18/35	LVDS1_D3_N	MIPI_CSI2_D3N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S19/37	GPIO-J			
S20/39	LVDS1_D2_P	MIPI_CSI2_D2P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S21/41	LVDS1_D2_N	MIPI_CSI2_D2N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S22/43	GND			
S23/45	LVDS1_D1_P	MIPI_CSI2_D1P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S24/47	LVDS1_D1_N	MIPI_CSI2_D1N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S25/49	GND			
S26/51	LVDS1_D0_P	MIPI_CSI2_D0P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S27/53	LVDS1_D0_N	MIPI_CSI2_D0N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S28/55	GND			

S29/57	LVDS1_CLK_P	MIPI_CSI2_CLKP	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S30/59	LVDS1_CLK_N	MIPI_CSI2_CLKN	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S31/61	GND			
S32/63	LVDS0_D3_P	HDMI_AUXP	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S33/65	LVDS0_D3_N	HDMI_AUXN	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S34/67	GPIO-H	I2C4_SDA	Yes	Controlled by alternative pin function PCIE2_CLKREQ_B
S35/69	LVDS0_D2_P	PCIE2_RX_P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S36/71	LVDS0_D2_N	PCIE2_RX_N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S37/73	GND			
S38/75	LVDS0_D1_P	PCIE2_TX_P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S39/77	LVDS0_D1_N	PCIE2_TX_N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S40/79	GND			
S41/81	LVDS0_D0_P	PCIE2_CLK_P	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S42/83	LVDS0_D0_N	PCIE2_CLK_N	No	Non-standard pin allocation (the i.MX 8M does not have any LVDS interface).
S43/85	GND			
S44/87	LVDS0_CLK_P			
S45/89	LVDS0_CLK_N			
S46/91	I2C-A_SDA	I2C1_SDA	No	Controlled by alternative pin function I2C1_SDA. Signal must be I2C1_SDA since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S47/93	I2C-A_SCL	I2C1_SCL	No	Controlled by alternative pin function I2C1_SCL. Signal must be I2C1_SCL since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S48/95	I2C-B_SDA	I2C2_SDA	Yes	Controlled by alternative pin function I2C2_SDA **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S49/97	I2C-B_SCL	I2C2_SCL	Yes	Controlled by alternative pin function I2C2_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S50/99	HDMI/I2C-C_SDA	HDMI_DDC_SDA	No	**Note**: There is no pullup resistor on this signal.
S51/101	HDMI/I2C-C_SCL	HDMI_DDC_SCL	No	**Note**: There is no pullup resistor on this signal.
S52/103	TP_RST	I2C3_SDA	Yes	Controlled by alternative pin function I2C3_SDA **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply. Non-standard pin allocation
S53/105	TP_IRQ	I2C3_SCL	Yes	Controlled by alternative pin function I2C3_SCL **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.

				Non-standard pin allocation
S54/107	DISP_PWR_EN			
S55/109	BL_PWR_EN			
S56/111	BL_PWM			
S57/113	GND			
S58/115	LCD_R0			
S59/117	LCD_R1			
S60/119	LCD_R2			
S61/121	LCD_R3			
S62/123	LCD_R4			
S63/125	LCD_R5	SAI1_RXFS	Yes	Controlled by alternative pin function GPIO4_IO0
S64/127	LCD_R6	SAI1_RXC	Yes	Controlled by alternative pin function GPIO4_IO1
S65/129	LCD_R7	SAI1_MCLK	Yes	Controlled by alternative pin function GPIO4_IO20
S66/131	LCD_G0	SAI1_RXD0	Yes	Controlled by alternative pin function GPIO4_IO2
S67/133	LCD_G1	SAI1_RXD1	Yes	Controlled by alternative pin function GPIO4_IO3
S68/135	LCD_G2	SAI1_RXD2	Yes	Controlled by alternative pin function GPIO4_IO4
S69/137	LCD_G3	SAI1_RXD3	Yes	Controlled by alternative pin function GPIO4_IO5
S70/139	LCD_G4	SAI1_RXD4	Yes	Controlled by alternative pin function GPIO4_IO6
S71/141	LCD_G5	SAI1_RXD5	Yes	Controlled by alternative pin function GPIO4_IO7
S72/143	LCD_G6	SAI1_RXD6	Yes	Controlled by alternative pin function GPIO4_IO8
S73/145	LCD_G7	SAI1_RXD7	Yes	Controlled by alternative pin function GPIO4_IO9
S74/147	GND			
S75/149	LCD_B0	SAI1_TXD0	Yes	Controlled by alternative pin function GPIO4_IO12
151	Non existing pin			
153	Non existing pin			
155	Non existing pin			
S76/157	LCD_B1	SAI1_TXD1	Yes	Controlled by alternative pin function GPIO4_IO13
S77/159	LCD_B2	SAI1_TXD2	Yes	Controlled by alternative pin function GPIO4_IO14
S78/161	LCD_B3	SAI1_TXD3	Yes	Controlled by alternative pin function GPIO4_IO15
S79/163	LCD_B4	SAI1_TXD4	Yes	Controlled by alternative pin function GPIO4_IO16
S80/165	LCD_B5	SAI1_TXD5	Yes	Controlled by alternative pin function GPIO4_IO17
S81/167	LCD_B6	SAI1_TXD6	Yes	Controlled by alternative pin function GPIO4_IO18
S82/169	LCD_B7	SAI1_TXD7	Yes	Controlled by alternative pin function GPIO4_IO19
S83/171	LCD_CLK	SAI1_TXC	Yes	Controlled by alternative pin function GPIO4_IO11
S84/173	GPIO-G			
S85/175	LCD_HSYNC	SAI1_TXFS	Yes	Controlled by alternative pin function GPIO4_IO10
S86/177	LCD_VSYNC			
S87/179	LCD_ENABLE			
S88/181	GND			
S89/183	AIN_VREF			
S90/185	AIN7			
S91/187	AIN6			

S92/189	AIN5	MIPI_DSI_D3N	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S93/191	AIN4	MIPI_DSI_D3P	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S94/193	AIN3	MIPI_DSI_D2N	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S95/195	AIN2	MIPI_DSI_D2P	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S96/197	AIN1	MIPI_DSI_D1N	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S97/199	AIN0	MIPI_DSI_D1P	No	Non-standard pin allocation (the i.MX 8M does not have any analog inputs).
S98/201	GND			
S99/203	COM board specific	MIPI_DSI_D0N	No	
S100/205	COM board specific	MIPI_DSI_D0P	No	
S101/207	GND			
S102/209	COM board specific	MIPI_DSI_CLKN	No	
S103/211	COM board specific	MIPI_DSI_CLKP	No	
S104/213	GND			
S105/215	COM board specific	GPIO4-SD2_VSELECT	No	Do not connect to this pin. Internally connected to GPIO4, which is a signal controlling the voltage level (1.8V or 3.3V) of the uSDHC2 interface.
S106/217	COM board specific	PMIC_STBY_REQ	No	Do not connect to this pin. Internally it is connected to i.MX 8M signal PMIC_STBY_REQ.
S107/219	COM board specific	PMIC_ON_REQ	No	Do not connect to this pin. Internally it is connected to i.MX 8M signal PMIC_ON_REQ.
S108/221	COM board specific	RTC_RESET_B	No	Do not connect to this pin. Internally it is connected to PMIC signal RTC_RESET_B.
S109/223	COM board specific	POR_B	No	Do not connect to this pin. Internally it is connected to PMIC signal POR_B. This signal is also available indirectly on the JTAG debug interface connector.
S110/225	COM board specific	CLK_32K	No	32.768kHz clock signal from PMIC. If using this signal externally on the carrier board use a buffer to minimize load in the signal. Note that the voltage level is 1.8V.
S111/227	COM board specific			
S112/229	COM board specific	SAI5_RXD3	Yes	Controlled by alternative pin function GPIO3_IO24
S113/231	COM board specific	SAI5_RXD2	Yes	Controlled by alternative pin function GPIO3_IO23
S114/233	CSI_HSYNC	SAI5_RXD1	Yes	Controlled by alternative pin function GPIO3_IO22 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S115/235	CSI_VSYNC	SAI5_RXD0	Yes	Controlled by alternative pin function GPIO3_IO21 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S116/237	CSI_MCLK	SAI5_MCLK	Yes	Controlled by alternative pin function GPIO2_IO25 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S117/239	CSI_PCLK	SAI5_RXC	Yes	Controlled by alternative pin function GPIO3_IO20 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S118/241	GND			

S119/243	CSI_D0	SAI5_RXFS	Yes	Controlled by alternative pin function GPIO3_IO19 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S120/245	CSI_D1	SAI3_MCLK	Yes	Controlled by alternative pin function GPIO5_IO2 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S121/247	CSI_D2	SAI3_RXC	Yes	Controlled by alternative pin function GPIO4_IO29 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S122/249	CSI_D3	SAI3_RXD	Yes	Controlled by alternative pin function GPIO4_IO30 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S123/251	CSI_D4	SAI3_RXFS	Yes	Controlled by alternative pin function GPIO4_IO28 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S124/253	CSI_D5	SAI3_TXC	Yes	Controlled by alternative pin function GPIO5_IO0 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S125/255	CSI_D6	SAI3_TXD	Yes	Controlled by alternative pin function GPIO5_IO1 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S126/257	CSI_D7	SAI3_TXFS	Yes	Controlled by alternative pin function GPIO4_IO31 Non-standard pin allocation (the i.MX 8M does not have any parallel camera input).
S127/259	GND			
S128/261	CSI_D3_M	MIPI_CSI1_D3N	No	
S129/263	CSI_D3_P	MIPI_CSI1_D3P	No	
S130/265	GND			
S131/267	CSI_D2_M	MIPI_CSI1_D2N	No	
S132/269	CSI_D2_P	MIPI_CSI1_D2P	No	
S133/271	GND			
S134/273	CSI_D1_M	MIPI_CSI1_D1N	No	
S135/275	CSI_D1_P	MIPI_CSI1_D1P	No	
S136/277	GND			
S137/279	CSI_D0_M	MIPI_CSI1_D0N	No	
S138/281	CSI_D0_P	MIPI_CSI1_D0P	No	
S139/283	GND			
S140/285	CSI_CLK_M	MIPI_CSI1_CLKN	No	
S141/287	CSI_CLK_P	MIPI_CSI1_CLKP	No	
S142/289	GND			
S143/291	SATA_TX_P			
S144/293	SATA_TX_N			
S145/295	GND			
S146/297	SATA_RX_N			
S147/299	SATA_RX_P			
S148/301	GND			

S149/303	GND			
S150/305	PCIE_CLK_P	PCIE1_CLK_P	No	If PCIe is used, connect to a 100MHz PCIe compatible reference clock with HCSL-signal output, positive signal
S151/307	PCIE_CLK_N	PCIE1_CLK_N	No	If PCIe is used, connect to a 100MHz PCIe compatible reference clock with HCSL-signal output, negative signal
S152/309	GND			
S153/311	PCIE_TX_P	PCIE_TX_P	No	
S154/313	PCIE_TX_N	PCIE_TX_N	No	
S155/315	GND			
S156/317	PCIE_RX_P	PCIE_RX_P	No	
S157/319	PCIE_RX_N	PCIE_RX_N	No	
S158/321	GND			

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 8M SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like PCIe, MIPI-DSI, MIPI-CSI and USB. i.MX 8M pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX8M COM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M pin. For more information about the register settings, see the *i.MX 8M Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *i.MX 8M Application Processor Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the EACOM function allocation. The reset state is typically GPIO, ALT5 function, except for the GPIO1_IO01-15 signals that are ALT0 functions, but that is the GPIO function.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M pin. For more information about the register settings, see the *i.MX 8M Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, with a 90Kohm pull-down resistor (a few has a 27Kohm pull-down or pull-up resistor instead), after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

This chapter lists details about all different interfaces. The **i.MX 8M datasheet and user manual should always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

Note that this chapter do not list all peripheral functions available on the i.MX 8M SoC. Only the ones related to the EACOM specification. For all available interfaces, consult *Chapter 8 - Chip IO and pinmux, Section 8.1 External Signals and Pin Multiplexing* in NXP's *i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors Reference Manual* (document id: IMX8MDQLQRM).

Example of peripheral blocks **not** listed in this chapter are listed below (see document IMX8MDQLQRM for details). Some of the blocks have multiple instances.

- CCM - Clock Controller Module
  Besides internal clocks, this peripheral can generate external clocks.
- GPMI - General Purpose Media Interface
  This peripheral provides a flexible interface to NAND flashes.
- SDMA - Smart Direct Memory Access Controller
  This peripheral provides fast data transfers between peripheral I/O devices and internal/external memories
- WDOG - Watchdog Timer
  This peripheral implements a watchdog timer.

There is an accompanying Excel document that lists all alternative functions for each available I/O pin.

5.1 Camera Interfaces

This section lists signals related to CMOS Sensor Interfaces (CSI). There are two camera interfaces. Both are serial (MIPI-CSI2) interfaces, supporting up to 4 data lanes and data rates between 80 Mbps and 1.5 Gbps. The interfaces support both dumb (supporting traditional VSYNC/HSYNC timing and Bayer data) and smart (supporting CCIR656 video decoder formats, with possible additional processing) image sensors.

The *EACOM Board specification* defines one serial camera interface. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S141/287	CSI_CLK_P	MIPI_CS1I_CLK0P	I	Positive D-Phy differential clock line Receiver input	
S140/285	CSI_CLK_N	MIPI_CSI1_CLK0N	I	Negative D-Phy differential clock line Receiver input	
S138/281	CSI_D0_P	MIPI_CSI1_D0P	I	Positive D-Phy differential data line Receiver input , Lane 0	
S137/279	CSI_D0_N	MIPI_CSI1_D0N	I	Negative D-Phy differential data line Receiver input , Lane 0	
S135/275	CSI_D1_P	MIPI_CSI1_D1P	I	Positive D-Phy differential data line Receiver input , Lane 1	
S134/273	CSI_D1_N	MIPI_CSI1_D1N	I	Negative D-Phy differential data line Receiver input , Lane 1	
S132/269	CSI_D2_P	MIPI_CSI1_D2P	I	Positive D-Phy differential data line Receiver input , Lane 2	
S131/267	CSI_D2_N	MIPI_CSI1_D2N	I	Negative D-Phy differential data line Receiver input , Lane 2	
S129/263	CSI_D3_P	MIPI_CSI1_D3P	I	Positive D-Phy differential data line Receiver input , Lane 3	
S128/261	CSI_D3_N	MIPI_CSI1_D3N	I	Negative D-Phy differential data line Receiver input , Lane 3	

The second serial camera interface is located on a non-standard location (according to the *EACOM Board specification*, since it only defines one serial camera interface). It is one of the EACOM LVDS interfaces that is used. The table below lists the pin assignment for the second serial camera interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S30/59	LVDS1_CLK_N	MIPI_CSI2_CLK0N	I	Negative D-Phy differential clock line Receiver input	Non-standard signal allocation
S29/57	LVDS1_CLK_P	MIPI_CS12_CLK0P	I	Positive D-Phy differential clock line Receiver input	Non-standard signal allocation
S27/53	LVDS1_D0_N	MIPI_CSI2_D0N	I	Negative D-Phy differential data line Receiver input , Lane 0	Non-standard signal allocation
S26/51	LVDS1_D0_P	MIPI_CSI2_D0P	I	Positive D-Phy differential data line Receiver input , Lane 0	Non-standard signal allocation
S24/47	LVDS1_D1_N	MIPI_CSI2_D1N	I	Negative D-Phy differential data line Receiver input , Lane 1	Non-standard signal allocation
S23/45	LVDS1_D1_P	MIPI_CSI2_D1P	I	Positive D-Phy differential data line Receiver input , Lane 1	Non-standard signal allocation
S21/41	LVDS1_D2_N	MIPI_CSI2_D2N	I	Negative D-Phy differential data line Receiver input , Lane 2	Non-standard signal allocation
S20/39	LVDS1_D2_P	MIPI_CSI2_D2P	I	Positive D-Phy differential data line Receiver input , Lane 2	Non-standard signal allocation
S18/35	LVDS1_D3_N	MIPI_CSI2_D3N	I	Negative D-Phy differential data line Receiver input , Lane 3	Non-standard signal allocation
S17/33	LVDS1_D3_P	MIPI_CSI2_D3P	I	Positive D-Phy differential data line Receiver input , Lane 3	Non-standard signal allocation

5.2 Display Interfaces

This section lists signals related to the two display output interfaces; HDMI and MIPI-DSI transmitter. Note specifically that the i.MX 8M SoC does not have a parallel RGB display output. HDMI and MIPI-DSI are the two available display outputs. An external MIPI-DSI to LVDS bridge can be used to connect to an LVDS display.

The picture below shows the high-level structure of the display interfaces. The picture comes from chapter 13 - Multimedia in the *i.MX 8M Application Processor Reference Manual* (IMX8MDQLQRM).

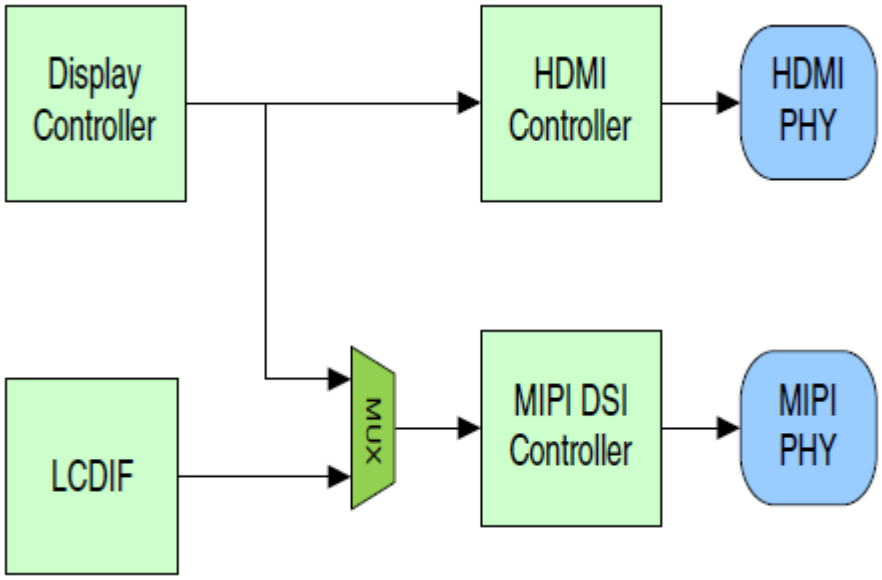


Figure 4 – Structure of Display Interfaces

5.2.1 HDMI Interface

This section lists signals for the High Definition Multimedia Interface - HDMI interface.

HDMI is capable of transferring uncompressed video, audio, and data with video pixel rates typically between 25 MHz and (up to) 600 MHz. HDMI uses Transition-minimized differential signaling (TMDS) with three data pairs and one clock pair. An optional Consumer Electronics Control (CEC) protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

The interface supports HDMI 1.4 and 2.0a specification as well as DisplayPort specification version 1.3. The interface further support CEA-861-F video formats, including 480p60, 720p60, 1080p60, 2160p60 (4k2k @ 60Hz).

Note that the I/O pins of the i.MX 8M are not 5V tolerant. In order not to damage the i.MX 8M SoC, and for proper functionality, the I2C, Hot Plug Detect and the CEC signals **must** be correctly level shifted.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P23/46	HDMI_TXC_N	HDMI_TX_M_LN_3	O	Differential clock pair, negative signal	
P24/48	HDMI_TXC_P	HDMI_TX_P_LN_3	O	Differential clock pair, positive signal	
P26/52	HDMI_TXD0_N	HDMI_TX_M_LN_0	O	Differential data pair #0, negative signal	
P27/54	HDMI_TXD0_P	HDMI_TX_P_LN_0	O	Differential data pair #0, positive signal	
P29/58	HDMI_TXD1_N	HDMI_TX_M_LN_1	O	Differential data pair #1, negative signal	
P30/60	HDMI_TXD1_P	HDMI_TX_P_LN_1	O	Differential data pair #1, positive signal	

P32/64	HDMI_TXD2_N	HDMI_TX_M_LN_2	O	Differential data pair #2, negative signal	
P33/66	HDMI_TXD2_P	HDMI_TX_P_LN_2	O	Differential data pair #2, positive signal	
P34/68	HDMI_CEC	HDMI_CEC	I/O	Consumer Electronics Control signal	**Note:** signal must be level shifted when connected to HDMI connector.
P28/56	HDMI_HPD	HDMI_HPD	I	Hot Plug Detect input	**Note:** signal must be level shifted when connected to HDMI connector.

The HDMI interface carries a VESA Data Display Channel (DDC). It is an I2C channel interface and the *EACOM Board specification* has allocated pins for this (I2C-C). The DDC is used for configuration and status exchange with the display.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S51/101	HDMI_DDC_SCL/ I2C-C_SCL	HDMI_DDC_SCL	I/O	HDMI DDC serial clock	**Note:** signal must be level shifted and have a pull-up resistor when connected to HDMI connector.
S50/99	HDMI_DDC_SDA/ I2C-C_SDA	HDMI_DDC_SDA	I/O	HDMI DDC serial data	**Note:** signal must be level shifted and have a pull-up resistor when connected to HDMI connector.

The i.MX 8M SoC HDMI interface also has a differential AUX channel. These two signals has a non-standard signal allocation (according to the *EACOM Board specification*) where two LVDS pins are used (since the i.MX 8M SoC does not have an LVDS interface).

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S32/63	LVDS0_D3_P	HDMI_AUX_P	I/O	AUX differential Tx/Rx serial data, positive signal	Non-standard signal allocation
S33/65	LVDS0_D3_N	HDMI_AUX_N	I/O	AUX differential Tx/Rx serial data, negative signal	Non-standard signal allocation

5.2.2 MIPI-DSI Interface

This section lists signals for the MIPI-DSI interface. The interface supports 4 data lanes with data rates between 80Mbps - 1.5Gbps. The data stream of pixels come from either the Display Controller or the LCDIF block.

The *EACOM Board specification* has no allocated pins for this interface so COM specific and non-standard signal allocation is used.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S103/211	COM specific	MIPI_DSI_CLK_P	O	Differential clock pair, positive signal	
S102/209	COM specific	MIPI_DSI_CLK_N	O	Differential clock pair, negative signal	
S100/205	COM specific	MIPI_DSI_D0_P	I/O	Differential data pair #0, positive signal	
S99/203	COM specific	MIPI_DSI_D0_N	I/O	Differential data pair #0, negative signal	
S97/199	AIN0	MIPI_DSI_D1_P	O	Differential data pair #1, positive signal	Non-standard signal allocation
S96/197	AIN1	MIPI_DSI_D1_N	O	Differential data pair #1, negative signal	Non-standard signal allocation
S95/195	AIN2	MIPI_DSI_D2_P	O	Differential data pair #2, positive signal	Non-standard signal allocation
S94/193	AIN3	MIPI_DSI_D2_N	O	Differential data pair #2, negative signal	Non-standard signal allocation

S93/191	AIN4	MIPI_DSI_D3_P	O	Differential data pair #3, positive signal	Non-standard signal allocation
S92/189	AIN5	MIPI_DSI_D3_N	O	Differential data pair #3, negative signal	Non-standard signal allocation

5.3 Digital Audio Interfaces

This section lists signals related to the Digital Audio Interfaces.

The i.MX 8M SoC has multiple audio interfaces, as listed below. The picture comes from chapter 13 - Multimedia in the *i.MX 8M Application Processor Reference Manual* (IMX8MDQLQRM).

Interface	Function	RX Data Line	TX Data Line	Note
SAI-1	External audio	8	8	
SAI-2	External audio	1	1	
SAI-3	External audio	1	1	
SAI-4	HDMI-TX	0	4	Internal connection
SAI-5	External audio	4	4	
SAI-6	External audio	1	1	
SPDIF-1	External audio	1	1	
SPDIF-2	HDMI ARC	1	0	Internal connection

Figure 5 – Audio Interfaces

5.3.1 Synchronous Audio Interface (SAI)

The table below lists pins that have been allocated according to the *EACOM Board specification*. The SAI2 port is used with **synchronous** transmit and receive sections (meaning that transmit and receive share the clock and frame synch signals).

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S5/9	AUDIO_RXD	SAI2_RXD	I	Data receive signal	Alternative function SAI2_RXD
S6/11	AUDIO_TXC	SAI2_TXC	O	Transmit clock signal. Also work as Receive clock signal	Alternative function SAI2_TX_BCLK
S7/13	AUDIO_TXD	SAI2_TXD	O	Data transmit signal	Alternative function SAI2_TXD
S4/7	AUDIO_TXFS	SAI2_TXFS	O	Transmit Frame sync signal. Also work as Receive Frame sync signal	Alternative function SAI2_TX_SYNC
S8/15	AUDIO_MCLK	SAI2_MCLK	O	Clock output signal	Alternative function SAI2_MCLK

Besides the SAI port #2 signals allocated in the *EACOM Board specification* there are more (alternative) pins for the SAI2 interface. The table below lists these pins.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S2/3	MQS_LEFT	SAI2_RXC	I/O	Receive Bit Clock	Alternative function SAI2_ RX_BCLK
S1/1	MQS_RIGHT	SAI2_RXFS	I/O	Receive Frame Sync	Alternative function SAI2_RX_SYNC

The table below lists pins available for the SAI1 interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S65/129	LCD_R7	SAI1_MCLK	I/O	Audio Master Clock	Alternative function SAI1_MCLK

S64/127	LCD_R6	SAI1_RXC	I/O	Receive Bit Clock	Alternative function SAI1_RX_BCLK
S66/131	LCD_G0	SAI1_RXD0	I	Receive Data	Alternative function SAI1_RX_DATA00
S67/133	LCD_G1	SAI1_RXD1	I	Receive Data	Alternative function SAI1_RX_DATA01
S68/135	LCD_G2	SAI1_RXD2	I	Receive Data	Alternative function SAI1_RX_DATA02
S69/137	LCD_G3	SAI1_RXD3	I	Receive Data	Alternative function SAI1_RX_DATA03
S70/139	LCD_G4	SAI1_RXD4	I	Receive Data	Alternative function SAI1_RX_DATA04
S71/141	LCD_G5	SAI1_RXD5	I	Receive Data	Alternative function SAI1_RX_DATA05
S72/143	LCD_G6	SAI1_RXD6	I	Receive Data	Alternative function SAI1_RX_DATA06
S73/145	LCD_G7	SAI1_RXD7	I	Receive Data	Alternative function SAI1_RX_DATA07
S63/125	LCD_R5	SAI1_RXFS	I/O	Receive Frame Sync	Alternative function SAI1_RX_SYNC
S71/141	LCD_G5	SAI1_RXD5	I/O	Receive Frame Sync	Alternative function SAI1_RX_SYNC
S83/171	LCD_CLK	SAI1_TXC	I/O	Transmit Bit Clock	Alternative function SAI1_TX_BCLK
S65/129	LCD_R7	SAI1_MCLK	I/O	Transmit Bit Clock	Alternative function SAI1_TX_BCLK
S116/237	CSI_MCLK	SAI5_MCLK	I/O	Transmit Bit Clock	Alternative function SAI1_TX_BCLK
S75/149	LCD_B0	SAI1_TXD0	O	Transmit Data	Alternative function SAI1_TX_DATA00
S119/243	CSI_D0	SAI5_RXFS	O	Transmit Data	Alternative function SAI1_TX_DATA00
S76/157	LCD_B1	SAI1_TXD1	O	Transmit Data	Alternative function SAI1_TX_DATA01
S117/239	CSI_PCLK	SAI5_RXC	O	Transmit Data	Alternative function SAI1_TX_DATA01
S77/159	LCD_B2	SAI1_TXD2	O	Transmit Data	Alternative function SAI1_TX_DATA02
S115/235	CSI_VSYNC	SAI5_RXD0	O	Transmit Data	Alternative function SAI1_TX_DATA02
S78/161	LCD_B3	SAI1_TXD3	O	Transmit Data	Alternative function SAI1_TX_DATA03
S114/233	CSI_HSYNC	SAI5_RXD1	O	Transmit Data	Alternative function SAI1_TX_DATA03
S79/163	LCD_B4	SAI1_TXD4	O	Transmit Data	Alternative function SAI1_TX_DATA04
S113/231	COM Specific	SAI5_RXD2	O	Transmit Data	Alternative function SAI1_TX_DATA04
S73/145	LCD_G7	SAI1_RXD7	O	Transmit Data	Alternative function SAI1_TX_DATA04
S80/165	LCD_B5	SAI1_TXD5	O	Transmit Data	Alternative function SAI1_TX_DATA05
S69/137	LCD_G3	SAI1_RXD3	O	Transmit Data	Alternative function SAI1_TX_DATA05
S81/167	LCD_B6	SAI1_TXD6	O	Transmit Data	Alternative function SAI1_TX_DATA06
S82/169	LCD_B7	SAI1_TXD7	O	Transmit Data	Alternative function SAI1_TX_DATA07
S85/175	LCD_HSYNC	SAI1_TXFS	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC
S114/233	CSI_HSYNC	SAI5_RXD1	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC
S113/231	COM Specific	SAI5_RXD2	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC
S112/229	COM Specific	SAI5_RXD3	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC
S73/145	LCD_G7	SAI1_RXD7	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC

The table below lists pins available for the SAI3 interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S120/245	CSI_D1	SAI3_MCLK	I/O	Audio Master Clock	Alternative function SAI3_MCLK
S121/247	CSI_D2	SAI3_RXC	I/O	Receive Bit Clock	Alternative function SAI3_RX_BCLK
S122/249	CSI_D3	SAI3_RXD	I	Receive Data	Alternative function SAI3_RX_DATA00
S123/251	CSI_D4	SAI3_RXFS	I/O	Receive Frame Sync	Alternative function SAI3_RX_SYNC

S124/253	CSI_D5	SAI3_TXC	I/O	Transmit Bit Clock	Alternative function SAI3_TX_BCLK
S125/255	CSI_D6	SAI3_TXD	O	Transmit Data	Alternative function SAI3_TX_DATA00
S126/257	CSI_D7	SAI3_TXFS	I/O	Transmit Frame Sync	Alternative function SAI3_TX_SYNC

The table below lists the single pin available for the SAI4 interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S116/237	CSI_MCLK	SAI5_MCLK	I/O	Audio Master Clock	Alternative function SAI4_MCLK

The table below lists pins available for the SAI5 interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S65/129	LCD_R7	SAI1_MCLK	I/O	Audio Master Clock	Alternative function SAI5_MCLK
S8/15	AUDIO_MCLK	SAI2_MCLK	I/O	Audio Master Clock	Alternative function SAI5_MCLK
S120/245	CSI_D1	SAI3_MCLK	I/O	Audio Master Clock	Alternative function SAI5_MCLK
S116/237	CSI_MCLK	SAI5_MCLK	I/O	Audio Master Clock	Alternative function SAI5_MCLK
S64/127	LCD_R6	SAI1_RXC	I/O	Receive Bit Clock	Alternative function SAI5_RX_BCLK
S121/247	CSI_D2	SAI3_RXC	I/O	Receive Bit Clock	Alternative function SAI5_RX_BCLK
S117/239	CSI_PCLK	SAI5_RXC	I/O	Receive Bit Clock	Alternative function SAI5_RX_BCLK
S66/131	LCD_G0	SAI1_RXD0	I	Receive Data	Alternative function SAI5_RX_DATA00
S122/249	CSI_D3	SAI3_RXD	I	Receive Data	Alternative function SAI5_RX_DATA00
S115/235	CSI_VSYNC	SAI5_RXD0	I	Receive Data	Alternative function SAI5_RX_DATA00
S67/133	LCD_G1	SAI1_RXD1	I	Receive Data	Alternative function SAI5_RX_DATA01
S126/257	CSI_D7	SAI3_TXFS	I	Receive Data	Alternative function SAI5_RX_DATA01
S114/233	CSI_HSYNC	SAI5_RXD1	I	Receive Data	Alternative function SAI5_RX_DATA01
S68/135	LCD_G2	SAI1_RXD2	I	Receive Data	Alternative function SAI5_RX_DATA02
S124/253	CSI_D5	SAI3_TXC	I	Receive Data	Alternative function SAI5_RX_DATA02
S113/231	COM Specific	SAI5_RXD2	I	Receive Data	Alternative function SAI5_RX_DATA02
S69/137	LCD_G3	SAI1_RXD3	I	Receive Data	Alternative function SAI5_RX_DATA03
S125/255	CSI_D6	SAI3_TXD	I	Receive Data	Alternative function SAI5_RX_DATA03
S112/229	COM Specific	SAI5_RXD3	I	Receive Data	Alternative function SAI5_RX_DATA03
S63/125	LCD_R5	SAI1_RXFS	I/O	Receive Frame Sync	Alternative function SAI5_RX_SYNC
S123/251	CSI_D4	SAI3_RXFS	I/O	Receive Frame Sync	Alternative function SAI5_RX_SYNC
S119/243	CSI_D0	SAI5_RXFS	I/O	Receive Frame Sync	Alternative function SAI5_RX_SYNC
S83/171	LCD_CLK	SAI1_TXC	I/O	Transmit Bit Clock	Alternative function SAI5_TX_BCLK
S2/3	MQS_LEFT	SAI2_RXC	I/O	Transmit Bit Clock	Alternative function SAI5_TX_BCLK
S113/231	COM Specific	SAI5_RXD2	I/O	Transmit Bit Clock	Alternative function SAI5_TX_BCLK
S75/149	LCD_B0	SAI1_TXD0	O	Transmit Data	Alternative function SAI5_TX_DATA00
S5/9	AUDIO_RXD	SAI2_RXD	O	Transmit Data	Alternative function SAI5_TX_DATA00
S112/229	COM Specific	SAI5_RXD3	O	Transmit Data	Alternative function SAI5_TX_DATA00
S76/157	LCD_B1	SAI1_TXD1	O	Transmit Data	Alternative function SAI5_TX_DATA01
S4/7	AUDIO_TXFS	SAI2_TXFS	O	Transmit Data	Alternative function SAI5_TX_DATA01

S77/159	LCD_B2	SAI1_TXD2	O	Transmit Data	Alternative function SAI5_TX_DATA02
S6/11	AUDIO_TXC	SAI2_TXC	O	Transmit Data	Alternative function SAI5_TX_DATA02
S78/161	LCD_B3	SAI1_TXD3	O	Transmit Data	Alternative function SAI5_TX_DATA03
S7/13	AUDIO_TXD	SAI2_TXD	O	Transmit Data	Alternative function SAI5_TX_DATA03
S85/175	LCD_HSYNC	SAI1_TXFS	I/O	Transmit Frame Sync	Alternative function SAI5_TX_SYNC
S1/1	MQS_RIGHT	SAI2_RXFS	I/O	Transmit Frame Sync	Alternative function SAI5_TX_SYNC
S114/233	CSI_HSYNC	SAI5_RXD1	I/O	Transmit Frame Sync	Alternative function SAI5_TX_SYNC

The table below lists pins available for the SAI6 interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S82/169	LCD_B7	SAI1_TXD7	I/O	Audio Master Clock	Alternative function SAI6_MCLK
S73/145	LCD_G7	SAI1_RXD7	I/O	Audio Master Clock	Alternative function SAI6_MCLK
S79/163	LCD_B4	SAI1_TXD4	I/O	Receive Bit Clock	Alternative function SAI6_RX_BCLK
S70/139	LCD_G4	SAI1_RXD4	I/O	Receive Bit Clock	Alternative function SAI6_RX_BCLK
S80/165	LCD_B5	SAI1_TXD5	I	Receive Data	Alternative function SAI6_RX_DATA00
S71/141	LCD_G5	SAI1_RXD5	I	Receive Data	Alternative function SAI6_RX_DATA00
S81/167	LCD_B6	SAI1_TXD6	I/O	Receive Frame Sync	Alternative function SAI6_RX_SYNC
S72/143	LCD_G6	SAI1_RXD6	I/O	Receive Frame Sync	Alternative function SAI6_RX_SYNC
S79/163	LCD_B4	SAI1_TXD4	I/O	Transmit Bit Clock	Alternative function SAI6_TX_BCLK
S70/139	LCD_G4	SAI1_RXD4	I/O	Transmit Bit Clock	Alternative function SAI6_TX_BCLK
S80/165	LCD_B5	SAI1_TXD5	O	Transmit Data	Alternative function SAI6_TX_DATA00
S71/141	LCD_G5	SAI1_RXD5	O	Transmit Data	Alternative function SAI6_TX_DATA00
S81/167	LCD_B6	SAI1_TXD6	I/O	Transmit Frame Sync	Alternative function SAI6_TX_SYNC
S72/143	LCD_G6	SAI1_RXD6	I/O	Transmit Frame Sync	Alternative function SAI6_TX_SYNC

5.3.2 Sony/Philips Audio Interface (S/PDIF)

This section lists signals related to the Sony/Philips Digital Interface (SPDIF) function.

The i.MX 8M SoC has one SPDIF interface, which is a stereo transceiver that allows the processor to receive and transmit digital audio according to the AES/EBU IEC 60958 standard.

The *EACOM Board specification* defines one input and one output SPDIF interface. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S10/19	SPDIF_IN	SPDIF_RX	I	Input line	
S11/21	SPDIF_OUT	SPDIF_TX	O	Output line signal	

There is one additional pin for SPDIF that is available as an alternative pin. The below lists this alternative pin location.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P138/284	PWM	SPDIF_EXT_CLK	I	Clock signal input	Alternative function SPDIF_EXT_CLK

5.4 Ethernet

This section lists signals related to the Ethernet interface.

The i.MX 8M SoC has one Gigabit Ethernet controllers (10/100/1000Mbps) that supports Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav) and IEEE1588. There is one on-board 10/100/1000 Mbps Ethernet interface. Atheros AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver is used as PHY and is connected via the RGMII interface to the i.MX 8M SoC.

The *EACOM Board Specification* defines two Ethernet interfaces. The i.MX 8M SoC Ethernet interface is assigned to ETH1. ETH2 is left unconnected.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals plus three link indicator activity signals. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

EACOM Board Pin	EACOM Board Name	AR8031 Pin	I/O	Description	Remarks
P39/78	ETH1_TRXP0	AR8031 #1 pin 11	I/O	Media Dependent Interface	
P40/80	ETH1_TRXN0	AR8031 #1 pin 12	I/O	Media Dependent Interface	
P36/72	ETH1_TRXP1	AR8031 #1 pin 14	I/O	Media Dependent Interface	
P37/74	ETH1_TRXN1	AR8031 #1 pin 15	I/O	Media Dependent Interface	
P48/96	ETH1_TRXP2	AR8031 #1 pin 17	I/O	Media Dependent Interface	
P47/94	ETH1_TRXN2	AR8031 #1 pin 18	I/O	Media Dependent Interface	
P45/90	ETH1_TRXP3	AR8031 #1 pin 20	I/O	Media Dependent Interface	
P44/88	ETH1_TRXN3	AR8031 #1 pin 21	I/O	Media Dependent Interface	
P42/84	ETH1_LED_ACT	AR8031 #1 pin 23	O	LED indicator output	Signal toggles during TX/RX activity.
P43/86	ETH1_LED_LINK	AR8031 #1 pin 26	O	LED indicator output	Signal high when 100M link is active.
P41/82	ETH1_LED_LINK1000	AR8031 #1 pin 24	O	LED indicator output	Signal high when 1000M link is connected or active.
P53/106	ETH2_TRXP0				ETH2 interface not connected
P54/108	ETH2_TRXN0				ETH2 interface not connected
P50/100	ETH2_TRXP1				ETH2 interface not connected
P51/102	ETH2_TRXN1				ETH2 interface not connected
P62/124	ETH2_TRXP2				ETH2 interface not connected
P61/122	ETH2_TRXN2				ETH2 interface not connected
P59/118	ETH2_TRXP3				ETH2 interface not connected
P58/116	ETH2_TRXN3				ETH2 interface not connected
P56/112	ETH2_LED_ACT				ETH2 interface not connected
P57/114	ETH2_LED_LINK100				ETH2 interface not connected
P55/110	ETH2_LED_LINK1000				ETH2 interface not connected

The on-board PHY can be powered down in order to lower the power consumption to a minimum.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 (ETH1_TRXP2/ ETH1_TRXN2) and MDI3 (ETH1_TRXP3/ ETH1_TRXN3) can be left unconnected.

Below is a list of suggested magnetics for 10/100/1000 Mbps Gigabit Ethernet operation:

Vendor	P/N	Package	Temp	Configuration
HanRun	HR911060C	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Halo	HFJ11-1G02E	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Pulse Electronics (Recommended by Atheros)	H5007	24-pin SOIC-W	0 - 70° Celsius	HP Auto-MDIX
Halo	TG1G-S002NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	-40 - 85° Celsius	HP Auto-MDIX
Halo	TG1G-E012NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX

5.5 GPT

This section lists signals related to the General Purpose Timer (GPT) peripheral.

The GPT has a 32-bit up-counter. The timer counter value can be captured in a register using an event on an external pin. The capture trigger can be programmed to be a rising or/and falling edge. The GPT can also generate an event on the output compare pins and an interrupt when the timer reaches a programmed value.

The table below lists where the GPT signals are available (as alternative pin functions). Note that all instances of GPT blocks have limited number, or no, external signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S126/257	CSI_D7	SAI3_TXFS	I	GPT1_CLK	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative location for GPT1_CLK signal.
S122/249	CSI_D3	SAI3_RXD	O	GPT1_COMPARE1	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative pin function GPT1_COMPARE1.
S124/253	CSI_D5	SAI3_TXC	O	GPT1_COMPARE2	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative location for GPT1_COMPARE2.
S125/255	CSI_D6	SAI3_TXD	O	GPT1_COMPARE3	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative pin function GPT1_COMPARE3.
S123/251	CSI_D4	SAI3_RXFS	I	GPT1_CAPTURE1	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative pin function GPT1_CAPTURE1.
S121/247	CSI_D2	SAI3_RXC	I	GPT1_CAPTURE2	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel camera interface). Alternative pin function GPT1_CAPTURE2.
S53/105	TP_IRQ	I2C3_SCL	I	GPT2_CLK	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel RGB display interface). Alternative pin function GPT2_CLK. Note that signal has on-board 2.2Kohm pullup resistor.
S52/103	TP_RST	I2C3_SDA	I	GPT3_CLK	Non-standard pin allocation (because the i.MX 8M SoC does not have a parallel RGB display interface). Alternative pin function GPT3_CLK. Note that signal has on-board 2.2Kohm pullup resistor.

5.6 QSPI

This section lists signals related to the Quad Serial Peripheral Interface (QSPI).

The i.MX 8M SoC can interface one, or two, external serial flash devices, each with up to four bidirectional data lines.

The table below lists where the QSPI signals are available (as alternative pin functions) for instance A:

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P111/230	COM specific	NAND_CE0_B	O	Chip select signal: QSPIA_SS0_B	Alternative location for QSPIA_SS0_B signal.
P110/228	COM specific	NAND_CE1_B	O	Chip select signal: QSPIA_SS1_B	Alternative location for QSPIA_SS1_B signal.
P112/232	COM specific	NAND_ALE	O	Clock signal: QSPIA_SCLK	Alternative location for QSPIA_SCLK signal.
P109/226	COM specific	NAND_DATA00	I/O	Data bit #0: QSPIA_DATA[0]	Alternative location for QSPIA_DATA[0] signal.
P108/224	COM specific	NAND_DATA01	I/O	Data bit #1: QSPIA_DATA[1]	Alternative location for QSPIA_DATA[1] signal.
P107/222	COM specific	NAND_DATA02	I/O	Data bit #2: QSPIA_DATA[2]	Alternative location for QSPIA_DATA[2] signal.
P106/220	COM specific	NAND_DATA03	I/O	Data bit #3: QSPIA_DATA[3]	Alternative location for QSPIA_DATA[3] signal.
P105/218	COM specific	NAND_DQS	I	Data strobe input: QSPIA_DQS	Alternative location for QSPIA_DQS signal.

The table below lists where the QSPI signals are available (as alternative pin functions) for instance B:

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P103/214	COM specific	NAND_CE2_B	O	Chip select signal: QSPIB_SS0_B	Alternative location for QSPIB_SS0_B signal.
P102/212	COM specific	NAND_CE3_B	O	Chip select signal: QSPIB_SS1_B	Alternative location for QSPIB_SS1_B signal.
P104/216	COM specific	NAND_CLE	O	Clock signal: QSPIB_SCLK	Alternative location for QSPIB_SCLK signal.
P101/210	COM specific	NAND_DATA04	I/O	Data bit #0: QSPIB_DATA[0]	Alternative location for QSPIB_DATA[0] signal.
P100/208	COM specific	NAND_DATA05	I/O	Data bit #1: QSPIB_DATA[1]	Alternative location for QSPIB_DATA[1] signal.
P99/206	COM specific	NAND_DATA06	I/O	Data bit #2: QSPIB_DATA[2]	Alternative location for QSPIB_DATA[2] signal.
P98/204	COM specific	NAND_DATA06	I/O	Data bit #3: QSPIB_DATA[3]	Alternative location for QSPIB_DATA[3] signal.
P97/202	COM specific	NAND_RE_B	I	Data strobe input: QSPIB_DQS	Alternative location for QSPIB_DQS signal.

5.7 GPIOs

This section lists signals related to General Purpose Input/Output (GPIO) functionality.

Many pins have GPIO functionality that can be enabled (via pin multiplexing). All GPIO pins can be used to generate interrupts as well as be wakeup sources.

The *EACOM Board specification* defines only a few GPIOs and they are listed in the table below. The pins that cannot be configured as GPIOs are Ethernet, USB, PCIe, HDMI, MIPI-CSI and MIPI-DSI. I2C pins can be GPIOs (except I2C-A is used on-board) but note that I2C2 and I2C3 have 2.2Kohm on-board pull-up resistors.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P140/288	GPIO-A	GPIO1_IO06	I/O	GPIO	GPIO-A controlled by alternative pin function GPIO1_IO06.
P139/286	GPIO-B	GPIO1_IO07	I/O	GPIO	GPIO-B controlled by alternative pin function GPIO1_IO07.
P4/8	GPIO-C	SD2_RESET_B	I/O	GPIO	GPIO-C controlled by alternative pin function GPIO2_IO19.
P3/6	GPIO-D	SD2_CD_B	I/O	GPIO	GPIO-D controlled by alternative pin function GPIO2_IO12.
P2/4	GPIO-E	I2C4_SCL	I/O	GPIO	GPIO-E controlled by alternative pin function GPIO5_IO20.
P1/2	GPIO-F	SD2_WP	I/O	GPIO	GPIO-F controlled by alternative pin function GPIO2_IO20.
S84/173	GPIO-G				
S34/67	GPIO-H	I2C4_SDA	I/O	GPIO	GPIO-H controlled by alternative pin function GPIO5_IO21.
S19/37	GPIO-J				

5.8 I2C

This section lists signals related to the Inter-Integrated Circuit (I2C) interface.

The i.MX 8M SoC has four I2C interfaces. Two of these are assigned in the *EACOM Board Specification*. i.MX 8M I2C channel #1 is assigned to EACOM I2C channel A. I2C channel #2 is assigned to EACOM I2C channel B. I2C channel #3 and #4 are available on non-standard locations.

EACOM I2C channel C carry the HDMI DDC channel. Note that this I2C channel can only access the HDMI screen. No other I2C slaves should be connected to this I2C channel.

Pin assignment for I2C channel A cannot be changed since this channel is used on the *iMX8M COM board* (for PMIC and E2PROM communication). It is recommended not to change pin assignment since for EACOM I2C channel B and C (I2C channel #2 and #3, respectively) since these four pins all have 2.2Kohm pull-up resistors.

The table below lists the pin assignment as well as alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S47/93	I2C-A_SCL	I2C1_SCL	I/O	Clock signal of I2C channel #1	Signal has on-board 2.2Kohm pull-up resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S46/91	I2C-A_SDA	I2C1_SDA	I/O	Data signal of I2C channel #1	Signal has on-board 2.2Kohm pull-up resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S49/97	I2C-B_SCL	I2C2_SCL	I/O	Clock signal of I2C channel #2	Signal has on-board 2.2Kohm pull-up resistor.
S48/95	I2C-B_SDA	I2C2_SDA	I/O	Data signal of I2C channel #2	Signal has on-board 2.2Kohm pull-up resistor.
S51/101	HDMI DDC_SCL/ I2C-C_SCL	HDMI_DDC_SCL	O	Clock signal of HDMI DDC I2C channel	Note that signal does not have an on-board pull-up resistor.
S50/99	HDMI DDC_SDA/ I2C-C_SDA	HDMI_DDC_SDA	I/O	Data signal of HDMI DDC I2C channel	Note that signal does not have an on-board pull-up resistor.

i.MX 8M I2C interface #3 can are located on the following pins (as alternative functions).

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S53/105	TP_IRQ	I2C3_SCL	I/O	Clock signal of I2C channel #3	Signal has on-board 2.2Kohm pull-up resistor.
S52/103	TP_RST	I2C3_SDA	I/O	Data signal of I2C channel #3	Signal has on-board 2.2Kohm pull-up resistor.

i.MX 8M I2C interface #4 can are located on the following pins (as alternative functions).

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P2/4	GPIO-E	I2C4_SCL	I/O	Clock signal of I2C channel #4	Note that an external pull-up resistor is needed.
S34/67	GPIO-H	I2C4_SDA	I/O	Data signal of I2C channel #4	Note that an external pull-up resistor is needed.

5.9 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 8M SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the ARM Cortex-A53 cores and Cortex-M4 core. The SJC complies with JTAG TAP standards. The i.MX 8M SoC use the JTAG port for production, testing, and system debugging.

The JTAG signals are not available on the MXM3 edge connector. Instead the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

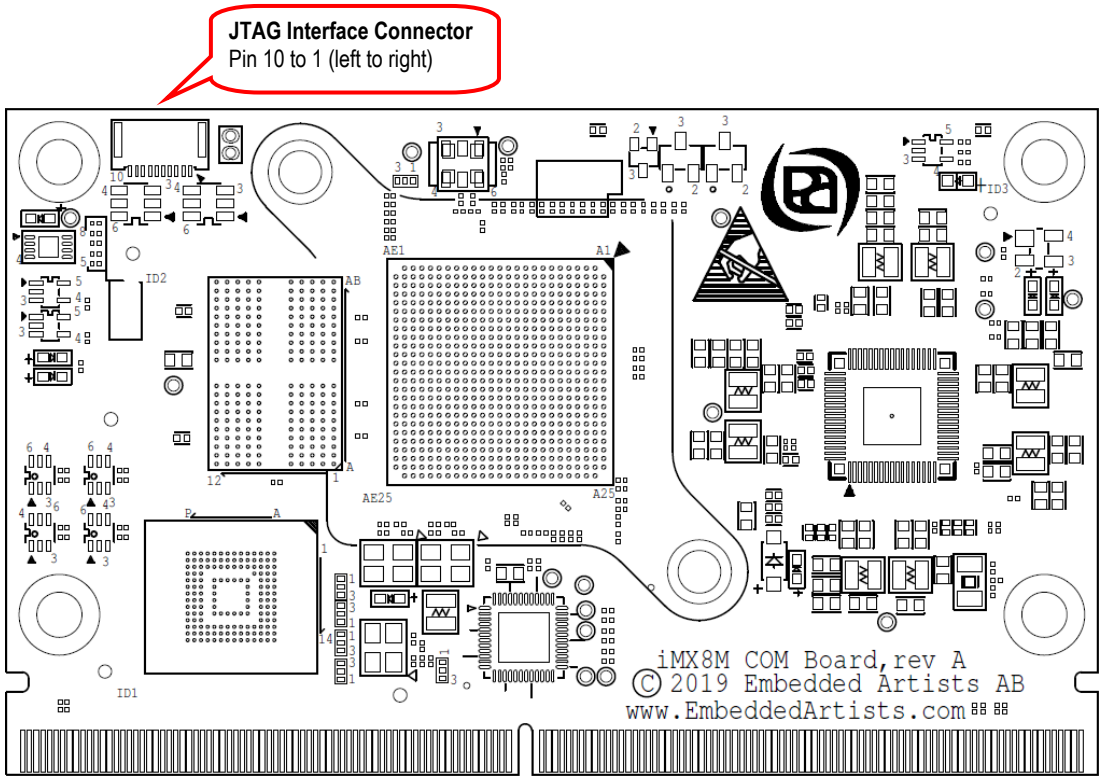


Figure 6 – iMX8M COM Board, Top Side

The table below lists the 10 signals on the JTAG connector.

J1 Pin Number	Connected to i.MX 8M Ball Name	I/O	Description	Remarks
1	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	Signal has a 10K ohm pull-down resistor.
5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 10Kohm pull-down resistor and can be left floating.
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	
10	JTAG_SRST	I	System reset	Signal is active low and controls internal system reset. Signal has a 10K ohm pull-up resistor.

There are on-board ESD protection of the JTAG interface, but it is still important to observe ESD precaution when connecting to this interface. There is no need for external pull-up or pull-down resistors.

The *iMX8M Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

5.10 PCI Express

This section lists signals related to the PCI Express interfaces.

The i.MX 8M SoC has dual single lane PCI Express (PCIe) interfaces. These interfaces are compliant with the PCIe 2.1 specification that supports up to 6Gbit/s data rate. PCIe 2.1/2.0 is backward compatible with the PCIe 1.1 standard that supports 2.5Gbit/s data rate.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S150/305	PCIE_CLK_P	PCIE1_CLK_P	I	100 MHz reference clock input, positive signal in differential pair	
S151/307	PCIE_CLK_N	PCIE1_CLK_N	I	100 MHz reference clock input, negative signal in differential pair	
S153/311	PCIE_TX_P	PCIE1_TX_P	O	Transmit data, positive signal in differential pair	
S154/313	PCIE_TX_N	PCIE1_TX_N	O	Transmit data, negative signal in differential pair	
S156/317	PCIE_RX_P	PCIE1_RX_P	I	Receive data, positive signal in differential pair	
S157/319	PCIE_RX_N	PCIE1_RX_N	I	Receive data, negative signal in differential pair	

The second PCIe interface is located on a non-standard location (according to the *EACOM Board specification*, since it only defines one PCIe interface). It is one of the EACOM LVDS interfaces that is used. The table below lists the pin assignment for the second PCIe interface.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S41/81	LVDS0_D0_P	PCIE2_CLK_P	I	100 MHz reference clock, positive signal in differential pair	Non-standard signal application
S42/83	LVDS0_D0_N	PCIE2_CLK_N	I	100 MHz reference clock, negative signal in differential pair	Non-standard signal application
S38/75	LVDS0_D1_P	PCIE2_TX_P	O	Transmit data, positive signal in differential pair	Non-standard signal application
S39/77	LVDS0_D1_N	PCIE2_TX_N	O	Transmit data, negative signal in differential pair	Non-standard signal application
S35/69	LVDS0_D2_P	PCIE2_RX_P	I	Receive data, positive signal in differential pair	Non-standard signal application
S36/71	LVDS0_D2_N	PCIE2_RX_N	I	Receive data, negative signal in differential pair	Non-standard signal application

When implementing a PCIe interface the clock request signal is typically also needed. This signal (individual to each PCIe interface) can be found on a couple of different places, see table below.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
S2/4	GPIO-E	I2C4_SCL	I/O	PCIE1_NCLKREQ	Select alternative pin function PCIE1_NCLKREQ
S34/67	GPIO-H	I2C4_SDA	I/O	PCIE2_NCLKREQ	Select alternative pin function PCIE2_NCLKREQ
P131/270	UART-B_CTS	UART4_RXD	I/O	PCIE1_NCLKREQ	Select alternative pin function PCIE1_NCLKREQ
P132/272	UART-B_RTS	UART4_TXD	I/O	PCIE2_NCLKREQ	Select alternative pin function PCIE2_NCLKREQ

5.11 Power Management

This section lists signals related to power management, i.e., reset and external power supplies.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P143/294	RESET_OUT	O	Reset output, active low	Open drain output. Driven low during reset. 1.5K pull-up resistor to an internally generated 3.3V supply.
P142/292	RESET_IN	I	Reset input, active low	Pull signal low to activate reset. No need to pull signal high externally. It is internally connected to the cathode of series diode, so logic level of driving signal can be anywhere between 1.5-5 V.
P141/290	PERI_PWR_EN	O	Enable signal (active high) for carrier board peripheral power supplies.	This output is connected to an internally generated 3.3V supply. When this supply is logically high (3.3V), external circuitry can also be powered. More information about carrier board design can be found in *EACOM Board specification*.

5.12 Power Supply Signals

This section lists signals related to power supply.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P147/302, P148/304, P149/306, P150/308, P151/310, P152/312, P153/314, P154/316, P155/318, P156/320	VIN	Pwr	4.2V supply voltage	See technical specification for details about valid range.
P22/44, P25/50, P31/62, P35/70, P38/76, P46/92, P49/98, P52/104, P60/120, P63/126, P69/138, P77/162, P82/172, P88/184, P91/190, P118/244, P127/262, S3/5, S9/17, S16/31, S22/43, S25/49, S28/55, S31/61, S37/73, S40/79, S43/85, S57/113, S74/147, S88/181, S98/201, S101/207, S104/213, S118/241, S127/259, S130/265, S133/271, S136/277, S139/283, S142/289, S145/295, S149/303, S152/309, S155/315, S158/321	GND	Pwr	Ground	
P145/298	VBAT-RTC	Pwr	Power supply for RTC and other low-power mode functionality.	See technical specification for details about valid range.
P144/296	VIN_SELECT	AO	VIN voltage range indicator	This output signals what input supply voltage (VIN) this COM board shall have. A logical low indicates 3.3V and a logical high (relative to VIN) indicates 4.2V (see technical specification for details about valid range). This output pin is connected to VIN via a 1Kohm resistor. Note that this pin is only of interest if the carrier board shall support other COM board (with VIN = 3.3V). It can be ignored if only iMX 8M COM board shall be supported.

5.13 PWM

This section lists signals related to Pulse Wide Modulators (PWM).

The i.MX 8M SoC has four PWM channels that are available via pin multiplexing. The generated signals has 16-bit resolution. PWM signals can be used to generate analogue signals (emulate a DAC) and also control intensity / brightness in display applications.

There are two PWM signals defined in the *EACOM Board specification*. One general PWM signal and one that is intended for backlight intensity control for displays. The general PWM signal is connected, but no signal has been connected to the the backlight intensity control.

The table below lists the pin assignment for the PWM signal and also the alternative pin locations for the other PWM signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P138/284	PWM	SPDIF_EXT_CLK	O	PWM1_OUT signal	Default PWM output in EACOM pinning.
P116/240	COM specific	GPIO1_IO01	O	PWM1_OUT signal	
S34/67	GPIO-H	I2C4_SDA	O	PWM1_OUT signal	
P74/148	USB_O1_OC	GPIO1_IO13	O	PWM2_OUT signal	
S10/19	SPDIF_IN	SPDIF_RX	O	PWM2_OUT signal	
P2/4	GPIO-E	I2C4_SCL	O	PWM2_OUT signal	
P75/158	USB_H1_PWR_EN	GPIO1_IO14	O	PWM3_OUT signal	
S11/21	SPDIF_OUT	SPDIF_TX	O	PWM3_OUT signal	
S52/103	TP_RST	I2C3_SDA	O	PWM3_OUT signal	
P76/160	USB_H1_OC	GPIO1_IO15	O	PWM4_OUT signal	
S120/245	CSI_D1	SAI3_MCLK	O	PWM4_OUT signal	
S53/105	TP_IRQ	I2C3_SCL	O	PWM4_OUT signal	

5.14 SD/MMC

This section lists signals related to Ultra Secured Digital Host Controller (uSDHC) functions.

The i.MX 8M SoC has two uSDHC interfaces. One, uSDHC1, is allocated (on-board) for interface to eMMC Flash. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 2.0/3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0/5.1
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0/3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The *EACOM Board specification* defines one 4-databit SD interface (SD) and one 8-databit MMC interface (MMC). uSDHC2 is connected to the SD interface. The MMC interface is unconnected since the i.MX 8M SoC does not have more uSDHC interfaces.

To support UHS-I (Ultra High Speed) SD cards, the I/O interface pins must drop from 3.3V to 1.8V operation. Signal SD2_VSELECT (available via pin GPIO1_IO04) is connected to the PMIC SD_VSELECT input, which allows the uSDHC2 signaling voltage to be either 3.3V or 1.8V. Note that when the uSDHC2 interface operates at 1.8V, all pins in this interface operates at 1.8V including card detect (SD2_CD), reset (SD2_RESET_B) and write protect (SD2_WP).

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P7/14	SD_CLK	SD2_CLK	O	Clock for MMC/SD/SDIO card	
P8/16	SD_CMD	SD2_CMD	I/O	CMD line connect to card	
P6/12	SD_D0	SD2_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P5/10	SD_D1	SD2_DATA1	I/O	DATA1 line in 4-bit mode. Also used to detect interrupt in 1/4-bit mode	
P10/20	SD_D2	SD2_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P9/18	SD_D3	SD2_DATA3	I/O	DATA3 line in 4-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	
P16/32	MMC_CLK				
P18/36	MMC_CMD				
P13/26	MMC_D0				
P12/24	MMC_D1				
P10/20	MMC_D2				
P20/40	MMC_D3				
P19/38	MMC_D4				
P17/34	MMC_D5				
P15/30	MMC_D6				
P14/28	MMC_D7				

The table below lists of alternative pin locations for uSDHC2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P4/8	GPIO-C	SD2_RESET_B	O	Reset signal, active low. Signal is used to power cycle the memory card interface.	Alternative function SD2_RESET_B **Note** that this pin can either be 3.3V or 1.8V logic level, depending on if the SD interface operates on 3.3V or 1.8V logic level.
P135/278	UART-A_CTS	GPIO1_IO08	O	Reset signal, active low. Signal is used to power cycle the memory card interface.	Alternative function SD2_RESET_B
P3/6	GPIO-D	SD2_CD_B	I	Card detection pin	Alternative function SD2_CD_B. **Note** that this pin can either be 3.3V or 1.8V logic level, depending on if the SD interface operates on 3.3V or 1.8V logic level.
P1/2	GPIO-F	SD2_WP	I	Card write protect detect	Alternative function SD2_WP **Note** that this pin can either be 3.3V or 1.8V logic level, depending on if the SD interface operates on 3.3V or 1.8V logic level.

There are no accessible pins for uSDHC1 signals since these are connected to the on-board eMMC Flash.

5.15 ECSPI / SPI

This section lists signals related to Enhanced Configurable Serial Peripheral Interface (ECSPI) functions.

The i.MX 8M SoC has 3 ECSPI block that are capable of full-duplex, synchronous, four-wire serial communication. The *EACOM Board specification* defines two 4-signal ECSPI interfaces. ECSPI1 and ECSPI2 have been allocated for these. The remaining ECSPI signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	ECSPI1_MISO	I/O	Master data in, slave data out	ECSPI1_MISO
P124/256	SPI-A_MOSI	ECSPI1_MOSI	I/O	Master data out, slave data in	ECSPI1_MOSI
P126/260	SPI-A_SCLK	ECSPI1_SCLK	I/O	SPI clock signal	ECSPI1_SCLK
P123/254	SPI-A_SS0	ECSPI1_SS0	I/O	Chip select signal	ECSPI1_SS0
P121/250	SPI-B_MISO	ECSPI2_MISO	I/O	Master data in, slave data out	ECSPI2_MISO
P120/248	SPI-B_MOSI	ECSPI2_MOSI	I/O	Master data out, slave data in	ECSPI2_MOSI
P122/252	SPI-B_SCLK	ECSPI2_SCLK	I/O	SPI clock signal	ECSPI2_SCLK
P119/246	SPI-B_SS0	ECSPI2_SS0	I/O	Chip select signal	ECSPI2_SS0

The table below lists of alternative pin locations for ECSPI3 signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P130/268	UART-B_RXD	UART2_RXD	I/O	Master data in, slave data out	ECSPI3_MISO
P137/282	UART-A_TXD	UART1_TXD	I/O	Master data out, slave data in	ECSPI3_MOSI
P134/276	UART-A_RXD	UART1_RXD	I/O	SPI clock signal	ECSPI3_SCLK
P133/274	UART-B_TXD	UART2_TXD	I/O	Chip select signal	ECSPI3_SS0

5.16 UART

This section lists signals related to Universal Asynchronous Receiver/Transmitter (UART) functions.

The i.MX 8M SoC has 4 UARTs. The *EACOM Board specification* defines two 4-signal UARTs and one 2-signal UART. The remaining UART signals are available as alternative functions on certain pins.

Note that the chip-level IOMUX modifies the direction and routing of the UART signals based on whether the UART is operating in DCE mode or DTE mode. See section 16.2.2 in IMX8MDQLQRM for details. The EACOM pinning assumes DCE operation.

UART pin	DCE Mode (default)	DTE Mode
UART-x_TXD	Serial data from DCE to DTE. Is an output from the i.MX 8M.	Serial data from DCE to DTE Is an input to the i.MX 8M.
UART-x_RXD	Serial data from DTE to DCE Is an input to the i.MX 8M.	Serial data from DTE to DCE Is an output from the i.MX 8M.
UART-x_RTS	UARTx_RTS from DTE to DCE Is an input to the i.MX 8M.	UARTx_RTS from DTE to DCE Is an output from the i.MX 8M.
UART-x_CTS	UARTx_CTS from DCE to DTE Is an output from the i.MX 8M.	UARTx_CTS from DCE to DTE Is an input to the i.MX 8M.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P137/282	UART-A_TXD	UART1_TXD	I/O	UART1 Transmit Data	Alternative function is UART1_TXD.
P134/276	UART-A_RXD	UART1_RXD	I/O	UART1 Receive Data	Alternative function is UART1_RXD.
P136/280	UART-A_RTS	GPIO1_IO05	I/O	UART1 Request to Send	Alternative function is UART1_RTS_B.
P135/278	UART-A_CTS	GPIO1_IO08	I/O	UART1 Clear to Send	Alternative function is UART1_CTS_B.
P133/274	UART-B_TXD	UART2_TXD	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
P130/268	UART-B_RXD	UART2_RXD	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
P132/272	UART-B_RTS	UART4_TXD	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
P131/270	UART-B_CTS	UART4_RXD	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.
P129/266	UART-C_TXD	UART3_TXD	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
P128/264	UART-C_RXD	UART3_RXD	I/O	UART3 Receive Data	Alternative function is UART3_RXD.

There are no alternative pin locations for the UART1 and UART2 signals.

The table below lists of alternative pin locations for UART3 signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	ECSPI1_MOSI	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
P126/260	SPI-A_SCLK	ECSPI1_SCLK	I/O	UART3 Receive Data	Alternative function is UART3_RXD.
P123/254	SPI-A_SS0	ECSPI1_SS0	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P124/256	SPI-A_MOSI	ECSPI1_MISO	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.

The table below lists of alternative pin locations for UART4 signals.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P120/248	SPI-B_MOSI	ECSPI2_MOSI	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
P132/272	UART-B_RTS	UART4_TXD	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
P122/252	SPI-B_SCLK	ECSPI2_SCLK	I/O	UART4 Receive Data	Alternative function is UART4_RXD.
P131/270	UART-B_CTS	UART4_RXD	I/O	UART4 Receive Data	Alternative function is UART4_RXD.
P119/246	SPI-B_SS0	ECSPI2_SS0	I/O	UART4 Request to Send	Alternative function is UART4_RTS_B.
P121/250	SPI-B_MISO	ECSPI2_MISO	I/O	UART4 Clear to Send	Alternative function is UART4_CTS_B.

5.17 USB

This section lists signals related to the USB interfaces.

The *EACOM Board Specification* has one USB 3.0 OTG port, one USB 3.0 Host port and one USB 2.0 Host port. The i.MX 8M has two USB 3.0/2.0 OTG ports. USB 3.0 is backward compatible with USB 2.0. USB 3.0 supports super-speed (SS, 5 Gbit/s), highspeed (HS, 480 Mbit/s), full-speed (FS, 12 Mbit/s) and low-speed (LS, 1.5 Mbit/s) operations.

The carrier board must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P64/128	USB_O1_DN	USB1_DN	I/O	USB PHY Data, Negative Differential	
P65/130	USB_O1_DP	USB1_DP	I/O	USB PHY Data, Positive Differential	
P66/132	USB_O1_ID	USB1_ID	I	USB OTG ID pin	
P67/134	USB_O1_SSTXN	USB1_TX_N	AO	USB PHY 3.0 Transmit Data, Negative Differential	
P68/136	USB_O1_SSTXP	USB1_TX_P	AO	USB PHY 3.0 Transmit Data, Positive Differential	
P70/140	USB_O1_SSRXN	USB1_RX_N	AI	USB PHY 3.0 Receive Data, Negative Differential	
P71/142	USB_O1_SSRXP	USB1_RX_P	AI	USB PHY 3.0 Receive Data, Positive Differential	
P72/144	USB_O1_VBUS	USB1_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.
P73/146	USB_O1_PWR_EN	GPIO1_IO12	O	Enable external USB voltage supply. Active high output.	Alternative function is USB_OTG1_PWR
P74/148	USB_O1_OC	GPIO1_IO13	I	Signals an over-current condition on the USB voltage supply. Active low input.	Alternative function is USB_OTG1_OC
P75/158	USB_H1_PWR_EN	GPIO1_IO14	O	Enable external USB voltage supply. Active high output.	Alternative function is USB_OTG2_PWR
P76/160	USB_H1_OC	GPIO1_IO15	I	Signals an over-current condition on the USB voltage supply. Active low input.	Alternative function is USB_OTG2_OC
P78/164	USB_H1_DN	USB2_DN	I/O	USB PHY Data, Negative Differential	
P79/166	USB_H1_DP	USB2_DP	I/O	USB PHY Data, Positive Differential	
P80/168	USB_H1_SSTXN	USB2_TX_N	AO	USB PHY 3.0 Transmit Data, Negative Differential	
P81/170	USB_H1_SSTXP	USB2_TX_P	AO	USB PHY 3.0 Transmit Data, Positive Differential	
P83/174	USB_H1_SSRXN	USB2_RX_N	AI	USB PHY 3.0 Receive Data, Negative Differential	
P84/176	USB_H1_SSRXP	USB2_RX_P	AI	USB PHY 3.0 Receive Data, Positive Differential	
P85/178	USB_H1_VBUS	USB2_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.

Note that EACOM USB Host port #2 is not used (since the i.MX 8M SoC has 2 USB ports). Some other signals are connected to these pins in a non-standard way, see table below.

EACOM Board Pin	EACOM Board Name	i.MX 8M Ball Name	I/O	Description	Remarks
P86/180	USB_H2_PWR_EN	USB2_ID	I/O	USB OTG2 ID	Signal can optionally be used to create a OTG port of the *EACOM* USB Host post.
P87/182	USB_H2_OC	ONOFF signal, i.MX 8M ball W21	I	Not connected for USB functionality	Not standard pin allocation.
P89/186	USB_H2_DN				
P90/188	USB_H2_DP				

6 Boot Control

This chapter presents the different boot settings that the *iMX8M COM Board* supports. This chapter will only present how the different options are controlled. Other documents discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *iMX8M COM Board* supports booting (i.e., from where the i.MX 8M SoC starts downloading code to start executing from) from different sources:

1. On-board eMMC Flash, which is the default
2. USB OTG download (also called 'serial download')
3. Other sources, like external SD/MMC memory cards, etc.
   Note that the OTP fuses must be programmed to set the specific source.

Two signals controls the booting source/process, BOOT_CTRL and ISP_ENABLE, see table below:

Boot source	BOOT_CTRL	ISP_ENABLE
Boot from on-board eMMC The board boots according to the default settings of signals SAI1_RXD0 - SAI1_RXD7 and SAI1_TXD0 - SAI1_TXD7, which have been setup to boot from eMMC. Note that these signals may not be driven externally during just after reset. The reason why the pins must not be driven externally is that on-board resistors pull these signals high/low to select eMMC booting. Driving any of these signals can change this default behavior. **If any of the signals are driven externally the on-chip OTP fuses must be programmed to force eMMC booting instead**	LOW (grounded)	Floating
Boot according to OTP fuses • Any boot mode supported by the i.MX 8M SoC and the hardware connected to it can be selected. See *i.MX8M Applications Processor Reference Manual* for details about available sources and OTP fuse settings. • Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to override the default setting to boot from eMMC and to have OTP fuse settings controlling boot source instead. • Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery. • Note that *iMX8M COM Boards* are delivered without programmed on-chip OTP fuses. Users have full control over these. • Note that the board must be able to boot into at least USB_OTG (ISP_ENABLE pin grounded) because the OTP fuses must be programmed the first time.	Floating	Floating
USB OTG This is known as "Serial Download" or "Recovery" mode.	Do not care	LOW (grounded)

This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation. This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.		

To summarize:

1. **The *iMX8M COM board* is setup to boot from eMMC as default. If another source is needed, program the OTP fuses.** Leave signal ISP_ENABLE floating and BOOT_CTRL grounded for this mode.
2. **If using the default setup (boot from eMMC), make sure the boot control pins (SAI1_RXD0 - SAI1_RXD7 and SAI1_TXD0 - SAI1_TXD7) are not driven externally.**
3. If signal ISP_ENABLE is pulled low (grounded), the i.MX 8M SoC boots into USB OTG mode. This mode it typically used during development and also during production (when the program images shall be downloaded the first time).
4. To boot from OTG fuses, leave signal BOOT_CTRL floating.

7 Technical Specification

7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	5.5	V
VBAT	RTC supply voltage	-0.3	5.5	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO	0	3.6	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.4	4.2	5.0 50 10	V mV mV
VBAT	RTC supply voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC).	3.0	3.3	5.5	V
USB_xx_VBUS	USB VBUS signals		5	5.25	V

7.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

7.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see i.MX 8M Datasheet. The internal VDD operating point for GPIOs is 3.3V.

7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN. Maximum output voltage when active is 0.4V.

7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 10 uS minimum. The internal reset pulse will be 140-560 mS long, before the i.MX 8M boot process starts.

7.5 Power Consumption

There are several factors that determine power consumption of the *iMX8M COM Board*, like input voltage, operating temperature, LPDDR4 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

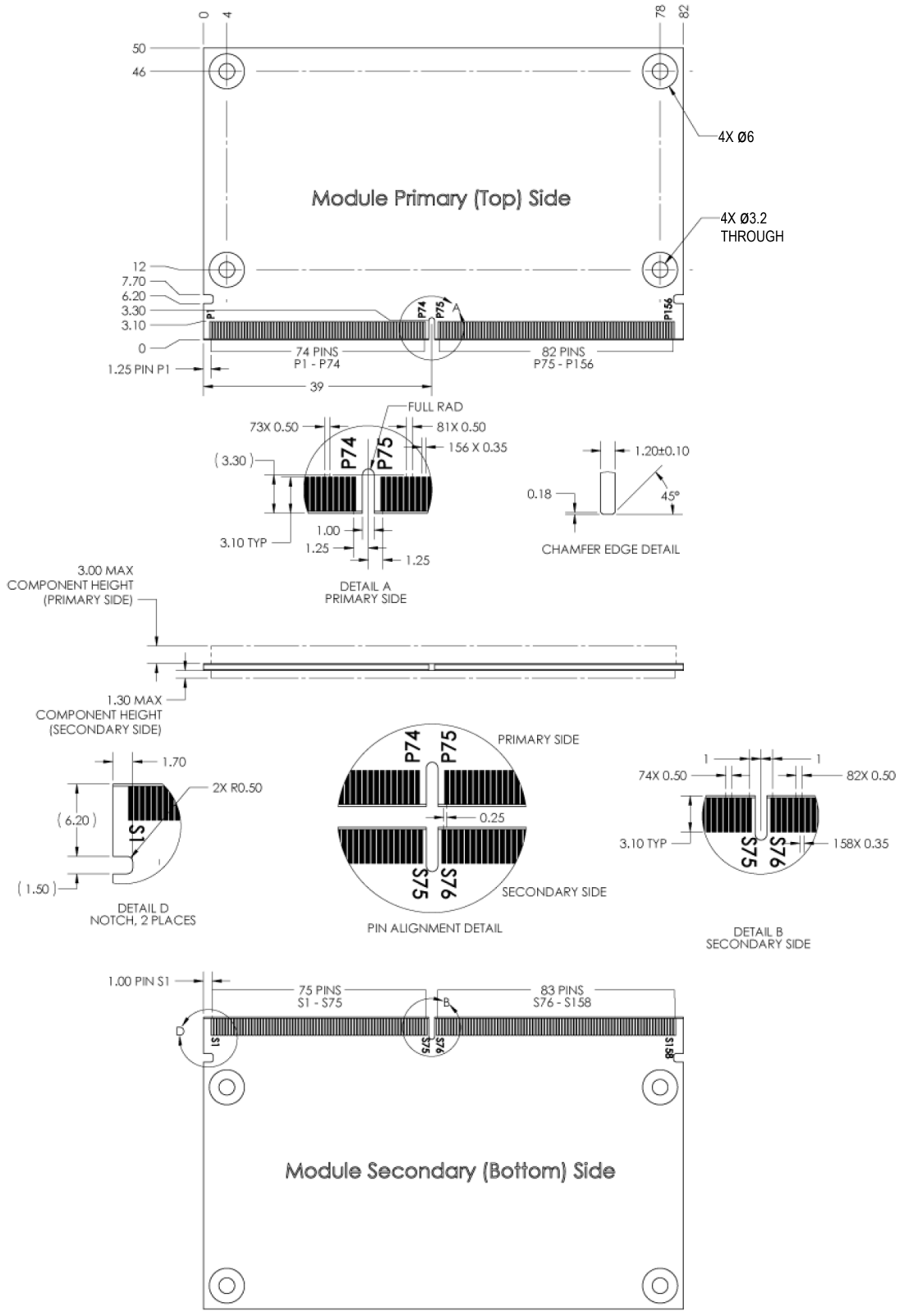
Symbol	Description (VIN = 4.2V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 1.5GHz ARM frequency, without Ethernet		TBD	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		TBD TBD TBD	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA
I_{VIN}_A7ACT	Android 7 Desktop active	TBD	TBD	mA
I_{VIN}_A7OFF	Android 7 Display off	TBD		mA

7.6 Mechanical Dimensions

The board use the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm
Module weight	16 ±1 gram	gram

The picture below show the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and show pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 7 – iMX8M COM Board Mechanical Outline

7.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE should not be used since this specific connector lack some of the pins. It is however possible to use the connector if it is acceptable for the project to not use the following pins:

- P146/300 ISP_ENABLE This pin is also used to select USB OTG as boot mode (when pulled low), also known as "factory recovery" mode. Not having access to this pin means that USB OTG mode cannot be enabled from the carrier board.
- P147/302 VIN This is not any problem since there are many VIN pins.
- S149/303 GND This is not any problem since there are many GND pins.
- S148/301 GND This is not any problem since there are many GND pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the COM Carrier board. This connector gives a board to board stacking height of 5.0 mm. This space allows some components to also be placed right under the COM board.

Always check available component height before placing components on the carrier board under the COM board, see picture below.

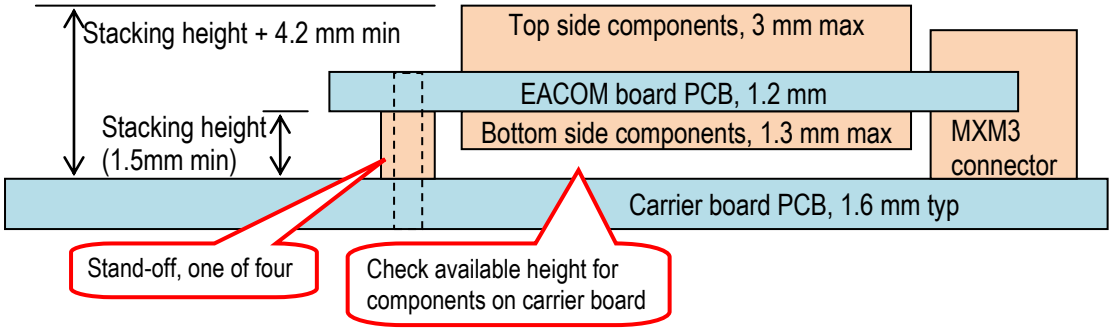


Figure 8 – COM Board Mounting in MXM3 Connector, Stacking Height

7.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

7.7 Environmental Specification

7.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature i.MX 8M SoC, operating:	comm. temp. range ind. temp. range.	0 -40	95 105	°C °C

[1] Depends on cooling/heat management solution.

7.7.2 Relative Humidity (RH)

Parameter		Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 70°C, non-condensing Operating: -40°C ≤ T_A ≤ 85°C, non-condensing	(comm. temp. range) (ind. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing		5	90	%

7.8 Thermal Design Considerations

Heat dissipation from the i.MX 8M SoC depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat can be up to 4 Watt in normal run mode.

External cooling will most likely be needed.

Note that no heat sink is shipped when ordering individual iMX8M COM Boards. Every application must evaluate what type of thermal management is needed and care must be taken not to exceed max junction temperature of the i.MX 8M SoC.

A heat sink is included as part of the iMX8M Developer's Kit. Type LPDR25-20B-0N0J1TL from www.alphanovatech.com is shipped. It is a heat sink suitable for natural convection or low air velocity. For more information, see http://www.alphanovatech.com/en/c_lpdr25e.html

Note that this heat sink may not be suitable for every application since air flow direction and heat dissipation needs might be different. There are two 3.175mm mounting holes (in the diagonal of a 30x30mm square) that allow for other heat sinks to be mounted.

Be very careful when mounting the heat sink. Do not apply force so that the PCB will bend. That will result in immediate failure of boards or long term reliability problems. **Apply equal counter-force on the bottom side - just where the holes are located - when pressing the push pins into the holes.**

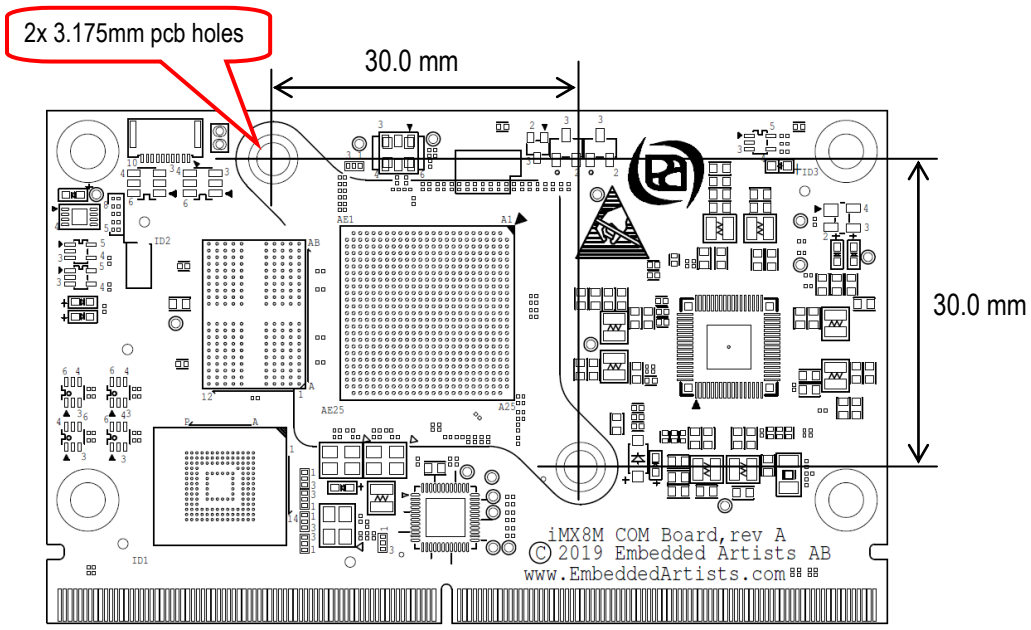


Figure 9 – iMX8M COM Board and Heat Sink Mounting

The i.MX 8M SoC and PMIC together implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this result in higher performance at lower average power consumption.

The .iMX 8M SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affect several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: AN12147, i.MX 8M Dual / 8M QuadLite / 8M Quad Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

7.8.1 Thermal Parameters

The i.MX 8M SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	16.4	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	0.1	°C/W

7.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

8 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the *iMX8M COM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX8M COM Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

9 Things to Note

This chapter presents a number of issues and considerations that users must note.

9.1 Shared Pins and Multiplexing

The i.MX 8M SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX8M COM* on-board design. Check if the needed interfaces are available to allocation before starting a design. See chapter 4 for details.

9.2 Use COM Carrier Board, rev E/E1 or Later

Only use rev E/E1 or later when using the iMX8M COM board. Earlier COM Carrier board versions do not support the 4.2V input supply voltage that is needed for the iMX8M COM board.

Note that rev E/E1 or later are also called "V2" iMX Developer's Kits.

9.3 COM Carrier Board Revision and HDMI Interface

Currently two version of the iMX8M COM board has been shipped, rev PA1 and rev A. Similarly there are two versions release of the COM Carrier board, rev E and rev E1. Of these four combinations, only the latest revision of each board will allow the HDMI DDC interface to work correctly, see table below:

Board revisions	**COM Carrier Board, rev E** HDMI DDC interface connected to I2C-B	**COM Carrier Board, rev E1** HDMI DDC interface connected to I2C-C
iMX8M COM board, rev PA1 HDMI DDC interface can optionally be connected to ETH2-TRX1	A rework on both the *iMX8M COM board* and *COM Carrier board* is required. On *iMX8M COM board*: mount zero ohm resistors (0402 size) on R188 and R189. On *COM Carrier board*: mount zero ohm resistors (0402 size) on R391 and R394. Remove resistors on R395 and R396. The HDMI DDC interface will be using two ETH2 pins. Note that the rework on the *COM Carrier board* will make it incompatible with other COM boards using the HDMI interface.	Not supported
iMX8M COM board, rev A HDMI DDC interface connected to I2C-C	A rework on the *iMX8M COM board* is required: place zero ohm resistors (0402 size) in 2-3 position of SJ2 and SJ3. The HDMI DDC interface will be using I2C-B interface. Note that after the rework, the M.2 I2C connection will no longer work (PCA expander and PCIe clock generator).	Will work out-of-the-box.

9.4 Only Use EA Board Support Package (BSP)

The *iMX8M COM board* use multiple on-board interfaces for the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX8M COM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

9.5 OTP Fuse Programming

The i.MX 8M SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 8M Datasheet* and *iMX 8M Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX8M COM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX8M COM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

9.6 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal ISP_ENABLE (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the i.MX 8M SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

9.7 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX8M COM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems

- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX8M COM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX8M COM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX8M COM Board*.

9.8 ESD Precaution when Handling iMX8M COM Board

Please note that the *iMX8M COM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

9.9 EMC / ESD

The *iMX8M COM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX8M COM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX8M COM Board*. ESD protection on board level is the same as what is specified in the i.MX 8M SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

10 Custom Design

This document specify the standard *iMX8M COM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *iMX8M COM Board* is integrated together with selected interfaces.
- Replace eMMC Flash with (unmanaged) MLC/SLC NAND Flash.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

11 Disclaimers

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