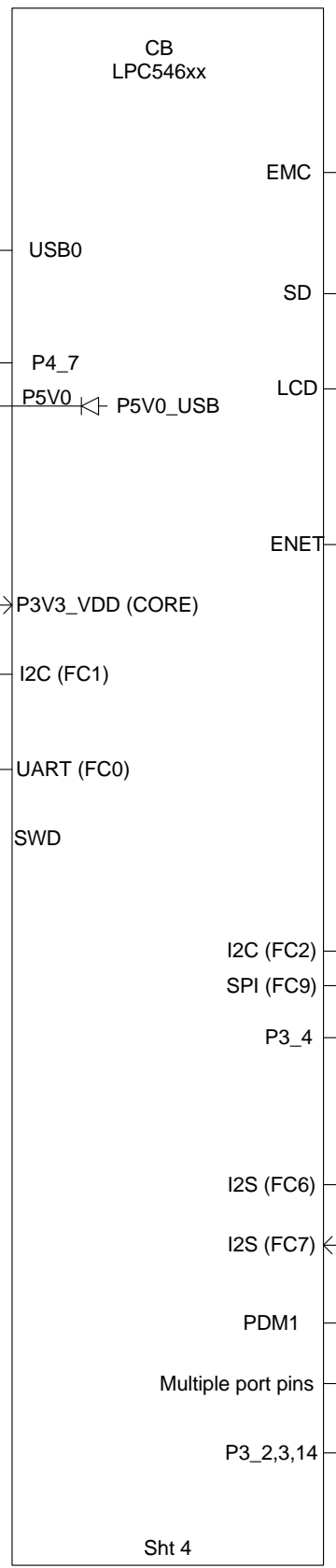


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	1st Schematic Review	08/6/2017	
1	RefDes re-order; release PCB	09/20/2017	

**Notes:**  
 1) "DNI" = Do Not Install by default  
 2) "JSx" solder jumpers use 0ohm resistor for default strapping.



# NXP Semiconductors

## LPC IoT Module Base Board

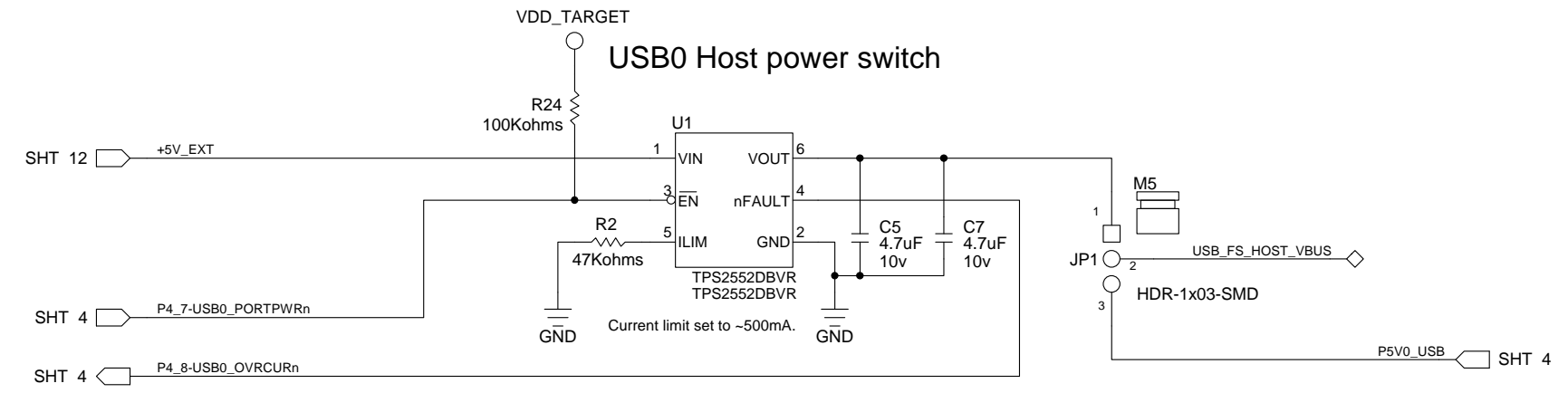
Sep 20, 2017

- Page 1 - Index / Block diagram
- Page 2 - Target LPC546xx FS USB
- Page 3 - Target LPC546xx Boot select / Accelerometer
- Page 4 - Target LPC546xx CB Interface connectors
- Page 5 - Target LPC546xx Current measurement / Link2 bridge
- Page 6 - Target EMC SDRAM
- Page 7 - LCD display + Cap touch / SD Card slot
- Page 8 - Ethernet PHY
- Page 9 - Audio Codec / DMIC
- Page 10 - Shield Receptacles / Pmod / User LEDs
- Page 11 - Debug LINK2 LPC4322 Peripherals / debug buffer
- Page 12 - Debug LINK2 LPC4322 / LINK2 USB / Board Power

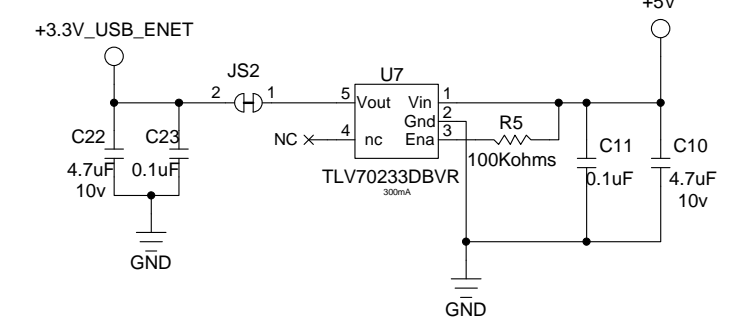
CONTRACT NO.		LPC IoT Module Basebrd Block Diagram	
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	9/20/2017		
CHECKED			
ISSUED	09/20/2017		
SIZE	D	DFSCM NO.	DWG. NO.
SCALE		LPC Treadstn Basebrd 1	
		SHEET 1 OF 12	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

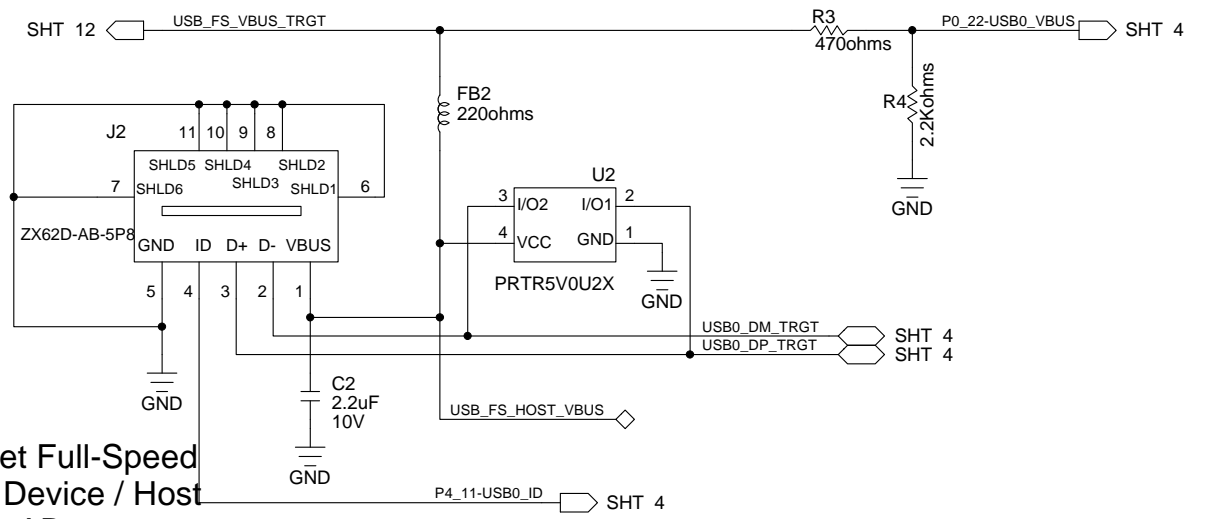
### USB0 Host power switch



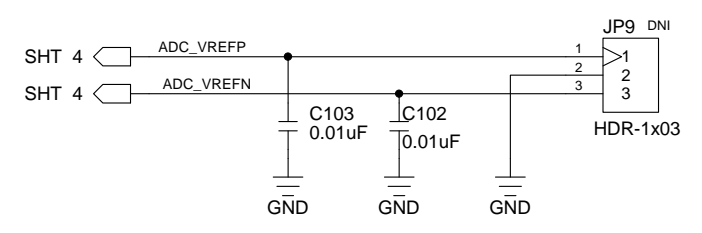
### Target USB HS / ENET+3.3V Power



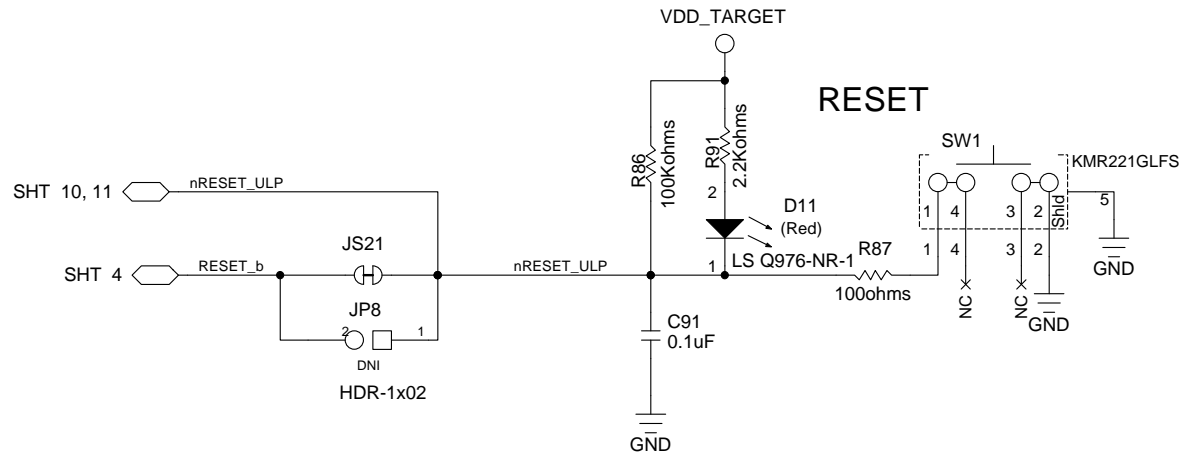
### Target Full-Speed USB Device / Host Micro-AB



### EXTERNAL ADC\_VREF

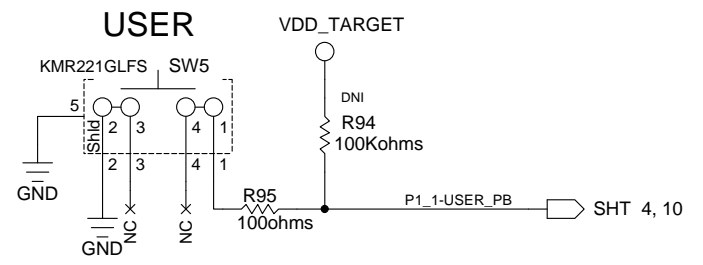
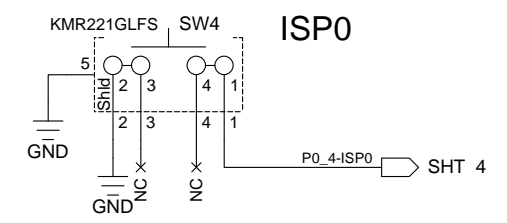
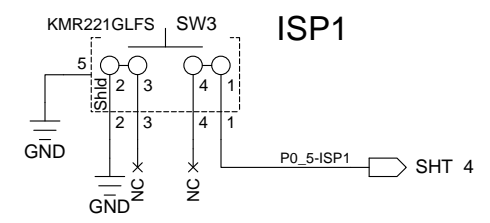
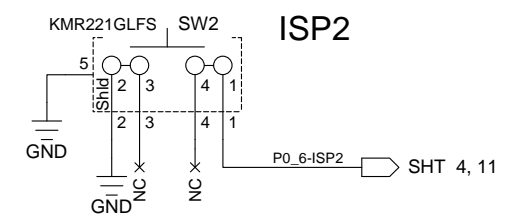
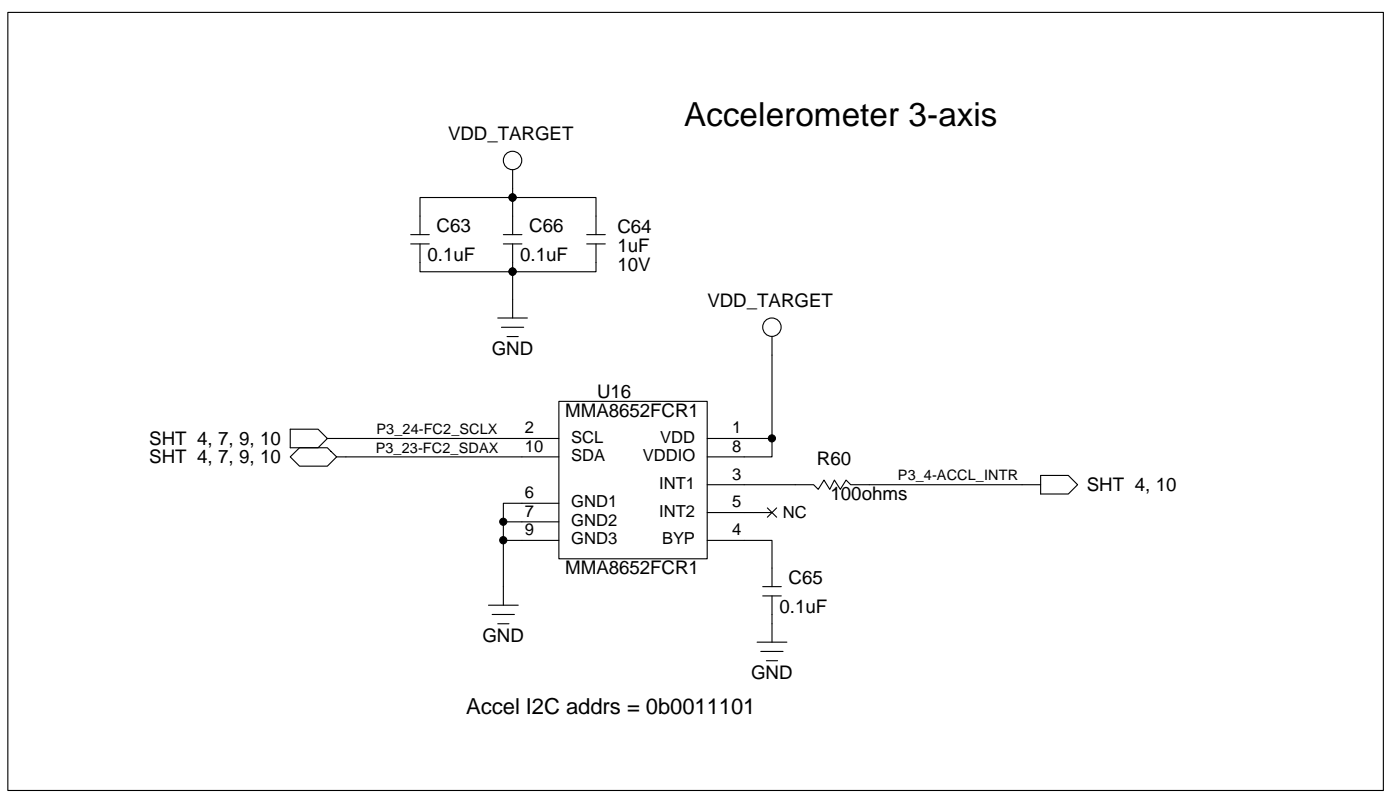


### RESET



CONTRACT NO.		Target LPC IoT Module FS USB	
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	9/20/2017		
CHECKED			
ISSUED	09/20/2017	SIZE	D
		FSCM NO.	
		DWG. NO.	LPC Treadstn Basebrd
		REV	1
		SCALE	SHEET 2 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

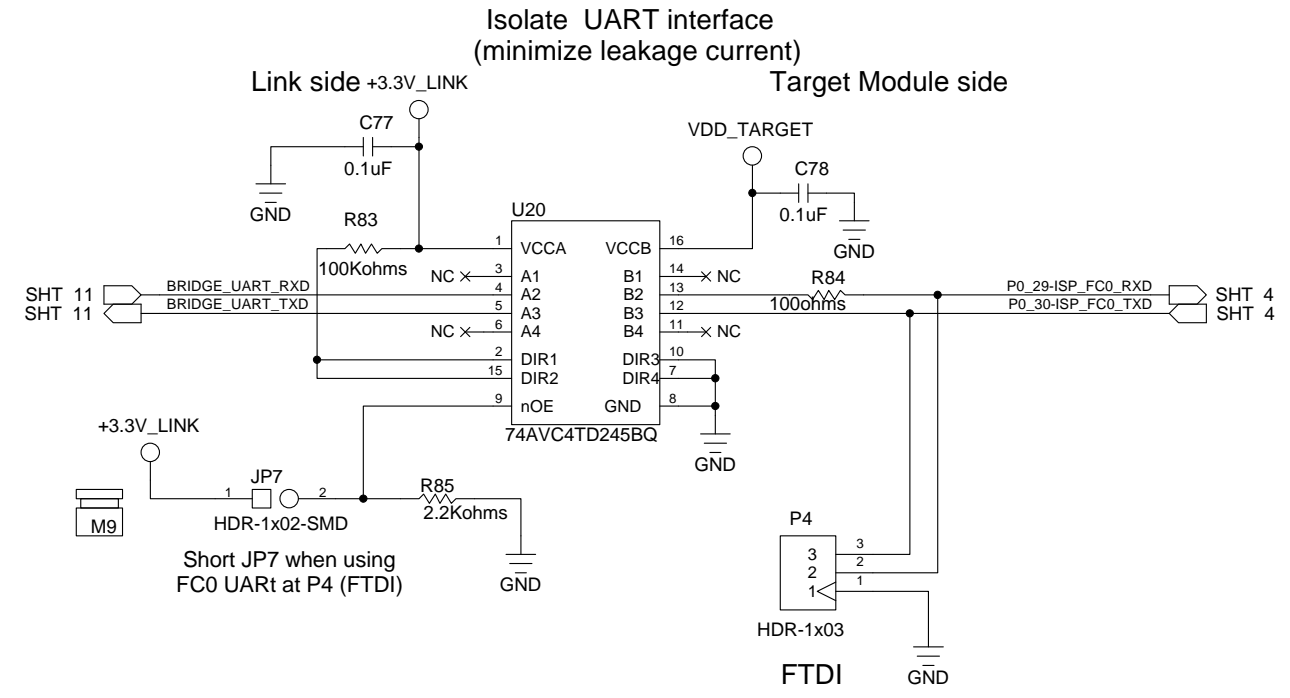
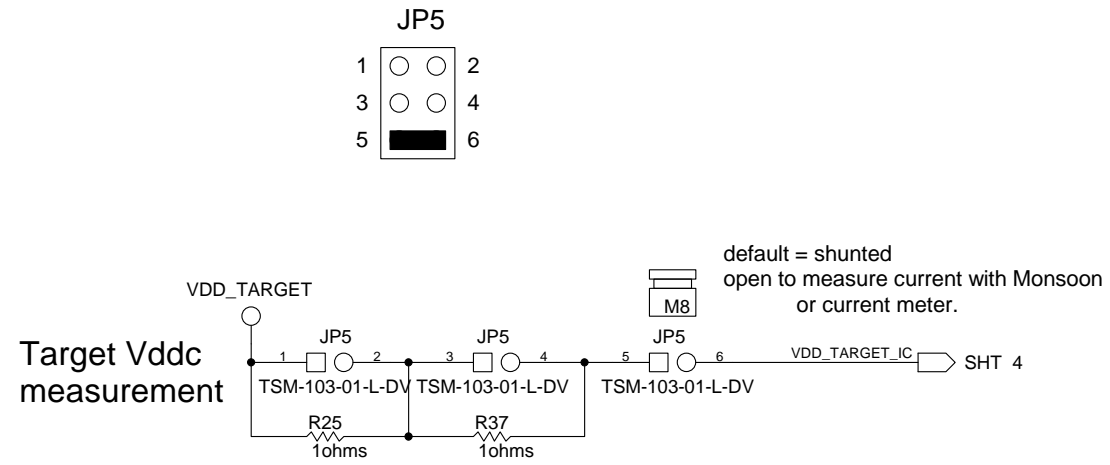


Target Module Boot (LPC54xxx)			
Mode	ISP2 P0_6	ISP1 P0_5	ISP0 P0_4
Internal Flash boot	high	high	high
ISP USB1 HS / QSP	low	high	high
ISP CAN	high	low	low
ISP USB0 FS	high	low	high
ISP UART/I2C/SPI	high	high	low

CONTRACT NO.		LPC IoT Module Boot select / Accelerometer			
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 <a href="http://www.standardics.nxp.com/microcontrollers/">www.standardics.nxp.com/microcontrollers/</a>			
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CHECKED					
ISSUED	09/20/2017				
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		D		LPC Treadstn Basebrd	1
		SCALE			SHEET 3 OF 12

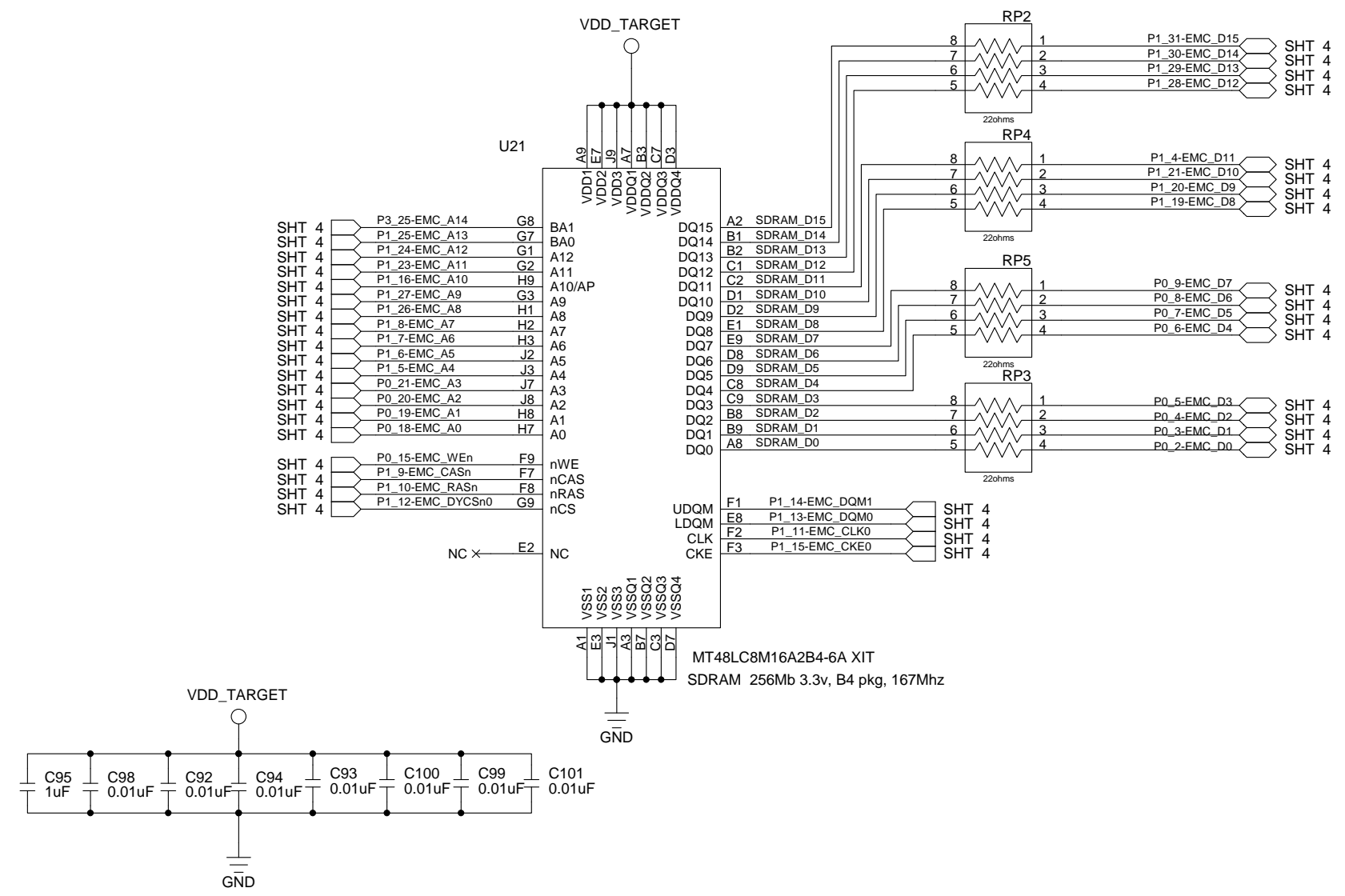


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



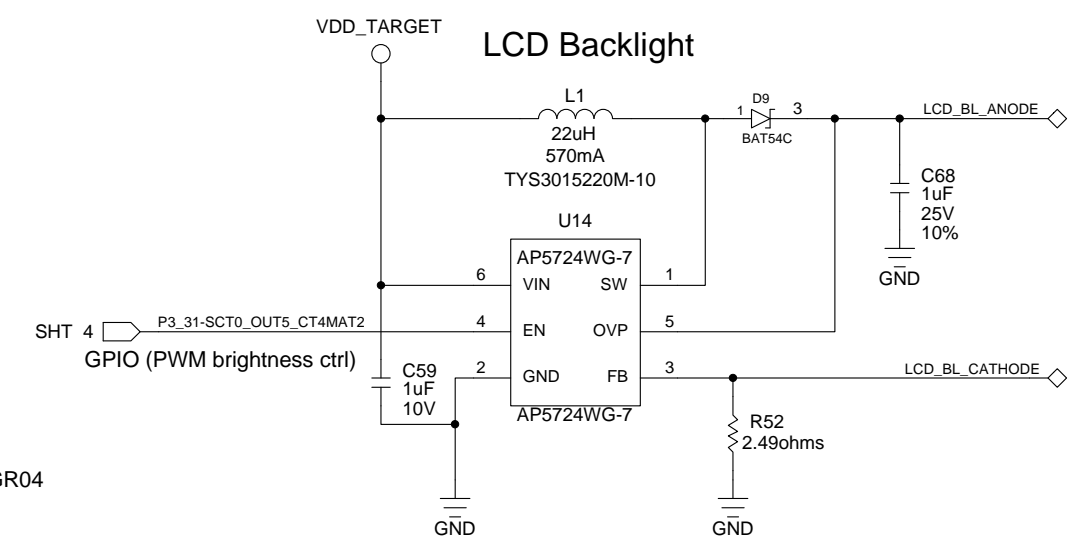
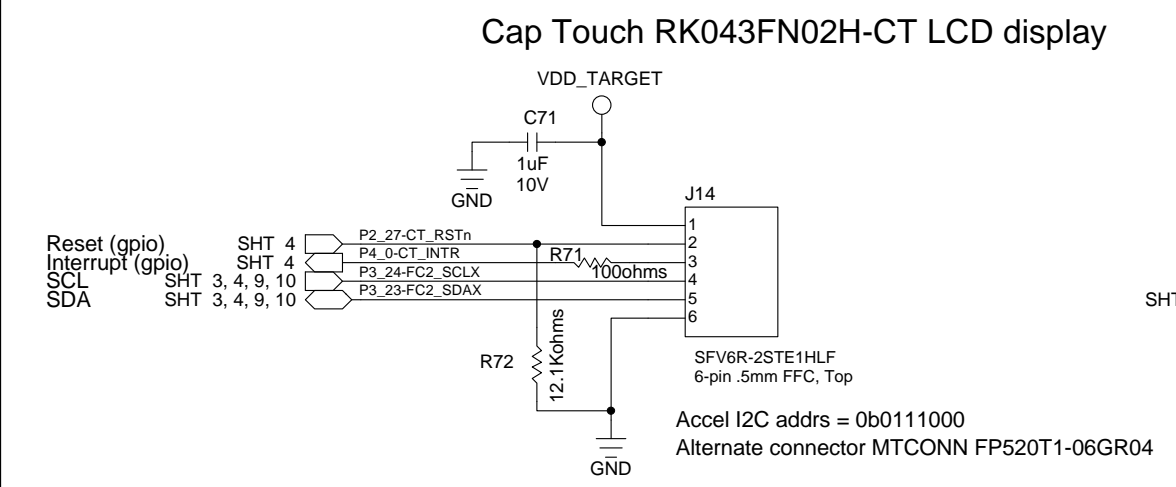
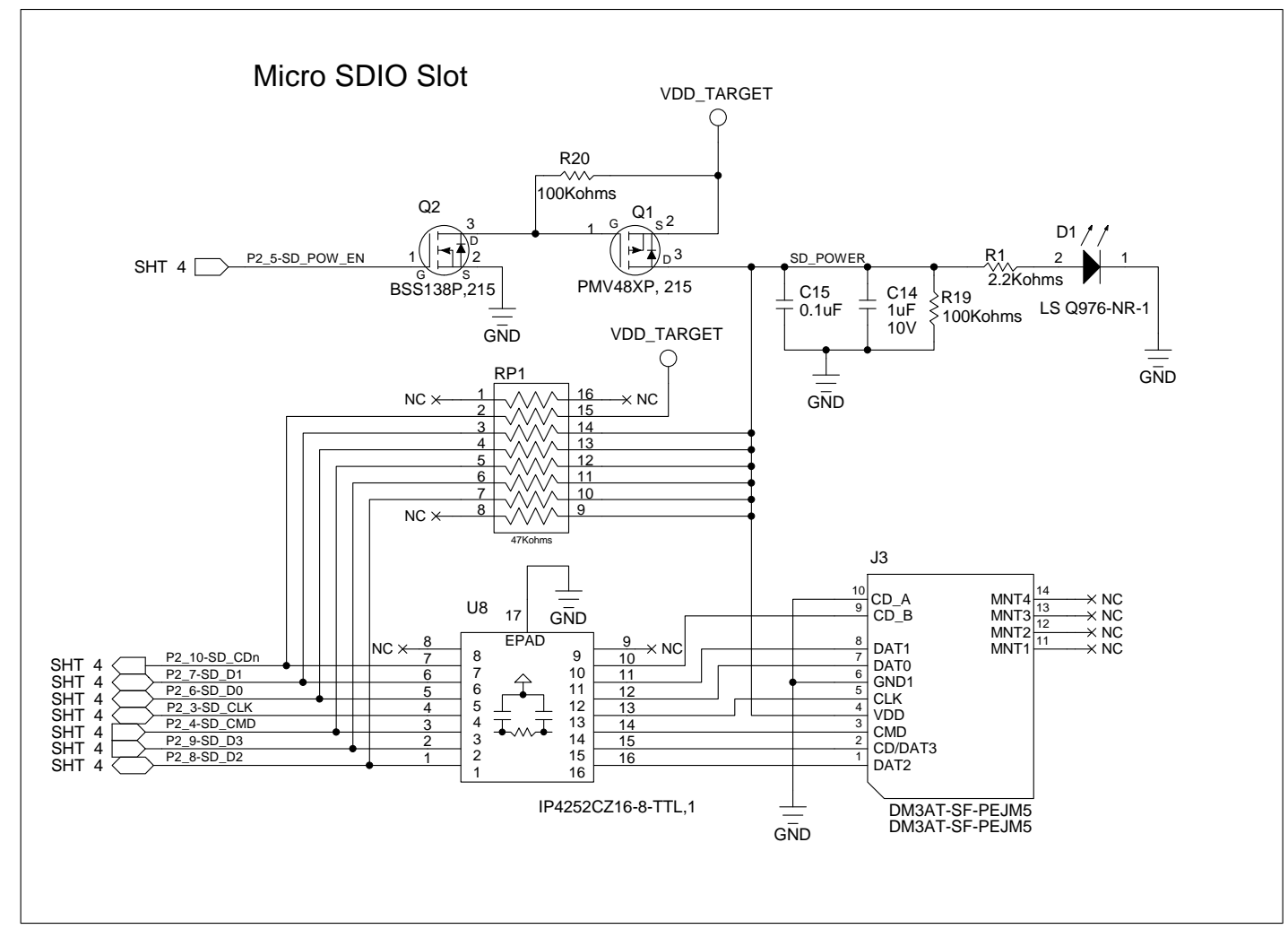
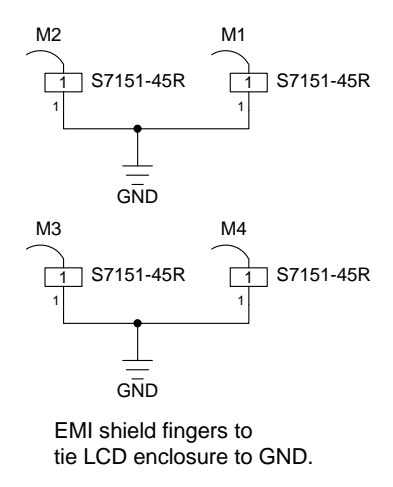
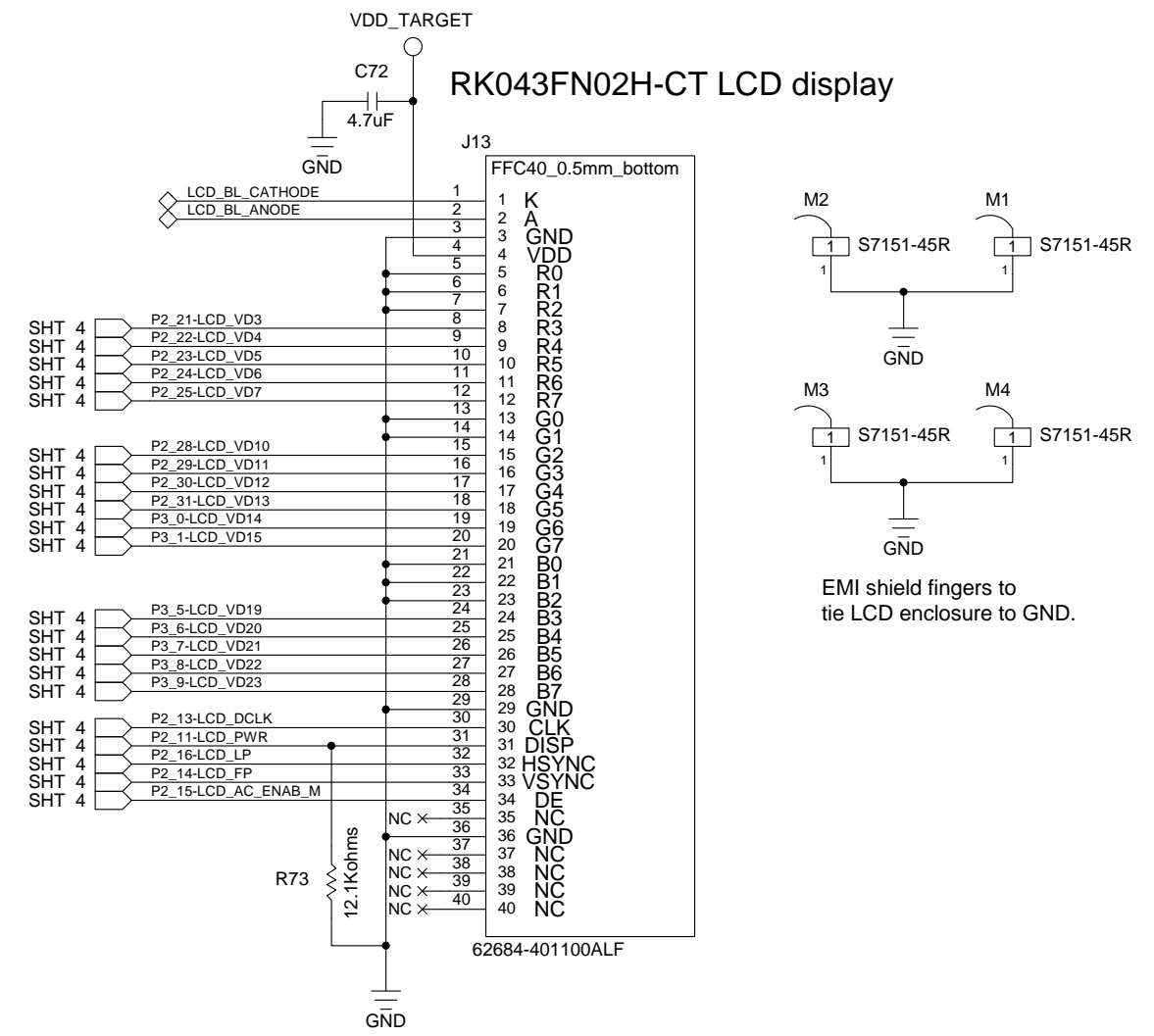
CONTRACT NO.		LINK2 Bridge buffer		
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 <a href="http://www.standardics.nxp.com/microcontrollers/">www.standardics.nxp.com/microcontrollers/</a>		
DRAWN	d.consiglio			9/20/2017
CHECKED				
ISSUED	09/20/2017	SIZE	D	
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		REV	1	
SCALE		SHEET	5 OF 12	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



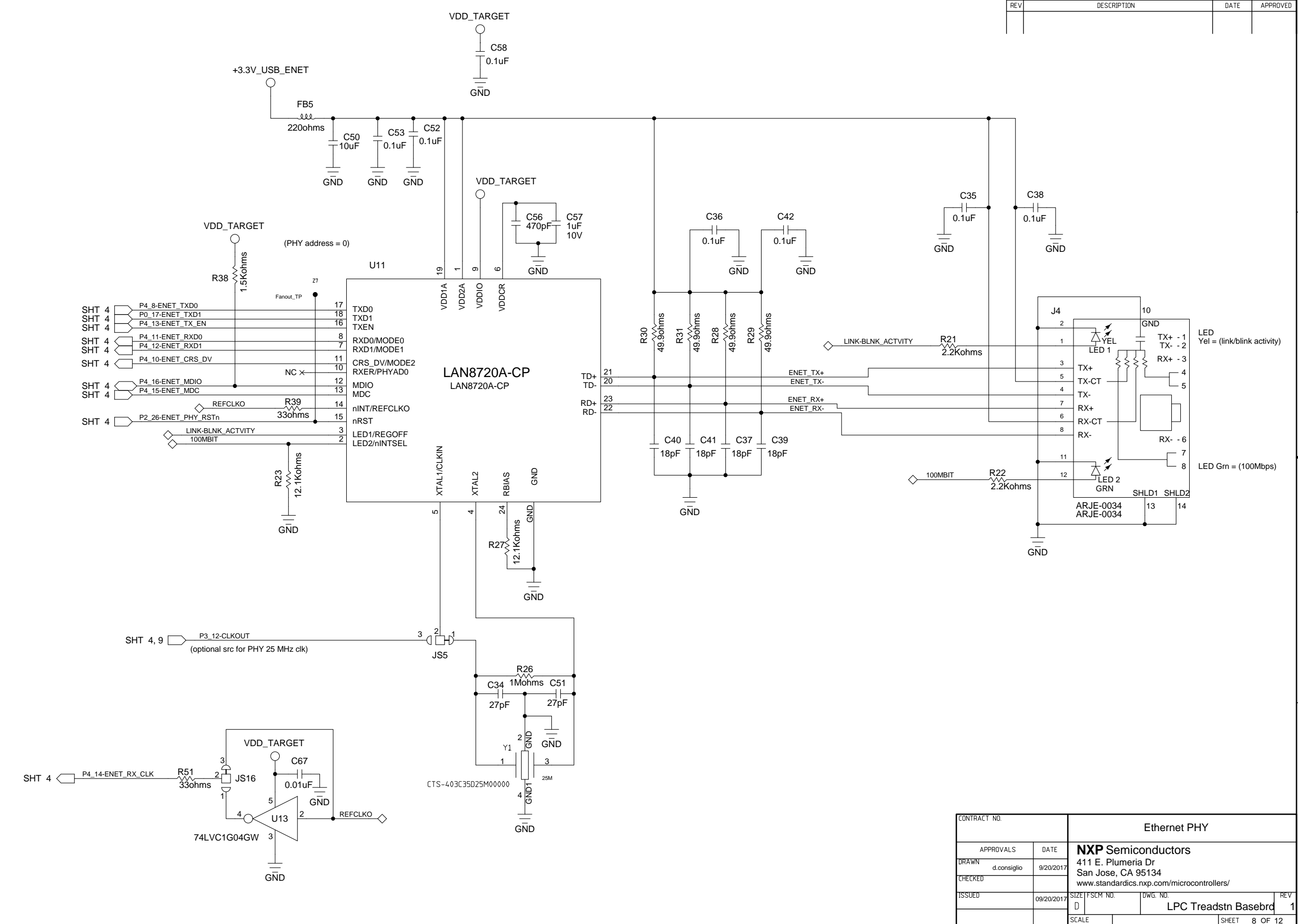
CONTRACT NO.		Target EMC SDRAM	
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 <a href="http://www.standardics.nxp.com/microcontrollers/">www.standardics.nxp.com/microcontrollers/</a>	
DRAWN	d.consiglio		
CHECKED			
ISSUED	09/20/2017	SIZE	D
		FSCM NO.	
		DWG. NO.	LPC Treadstn Basebrd
		REV	1
		SCALE	
		SHEET	6 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		LCD display + Cap touch / uSD Card slot	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	9/20/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE D	DWG. NO. LPC Treadstn Basebrd
ISSUED	09/20/2017	SCALE	REV 1
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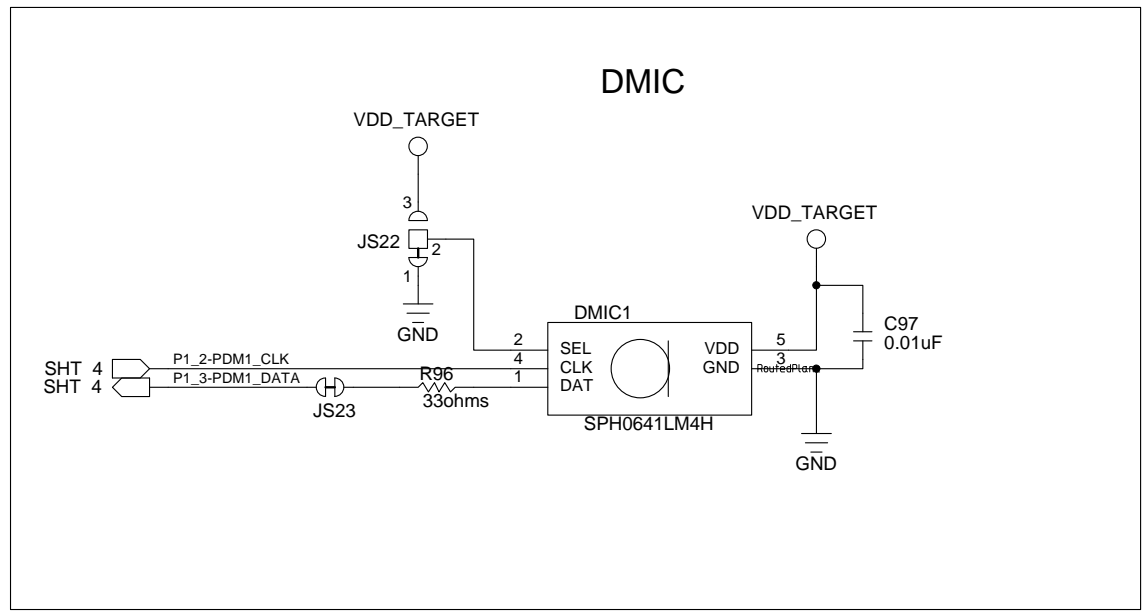
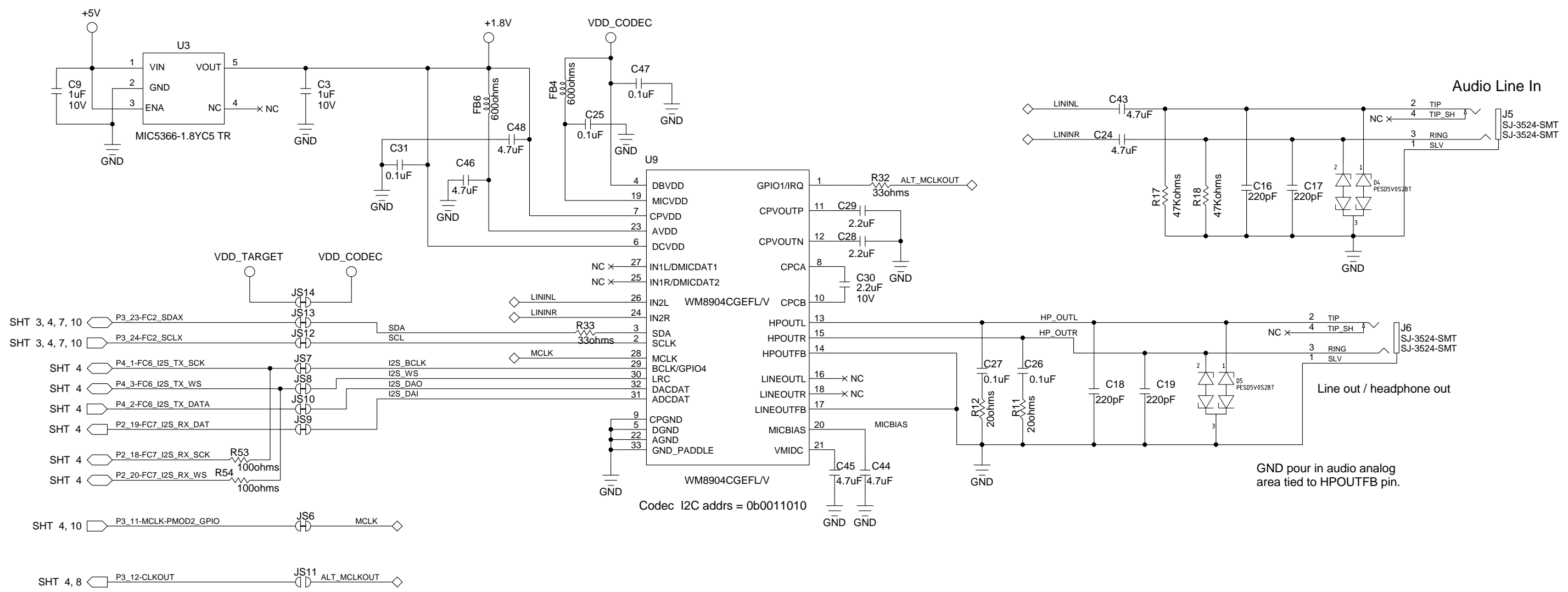
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Ethernet PHY	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	9/20/2017	San Jose, CA 95134	
ISSUED	09/20/2017	www.standardics.nxp.com/microcontrollers/	
		SIZE / FSCM NO.	DWG. NO.
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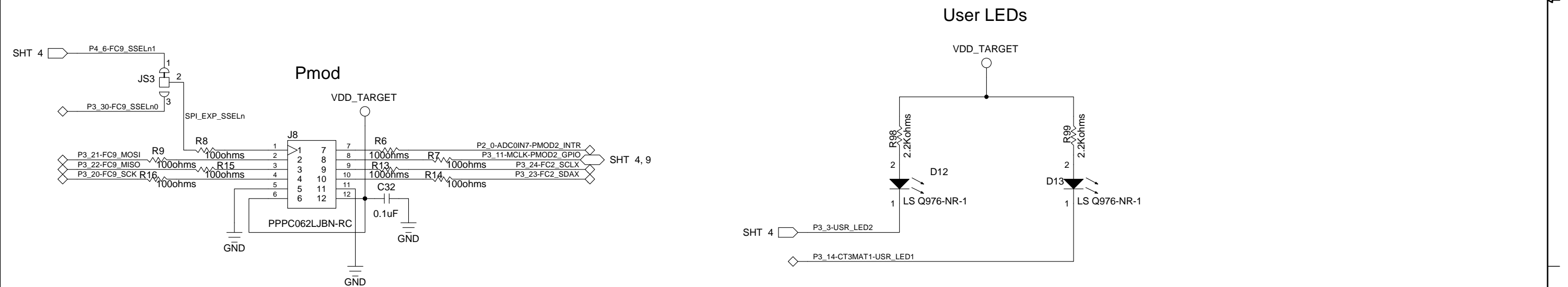
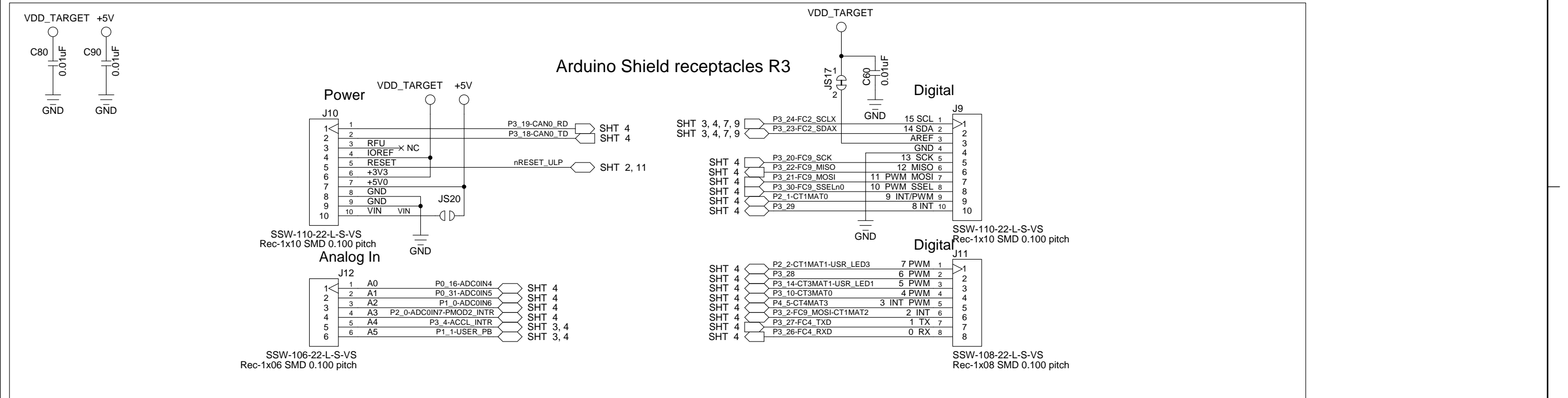


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REV	DESCRIPTION	DATE	APPROVED



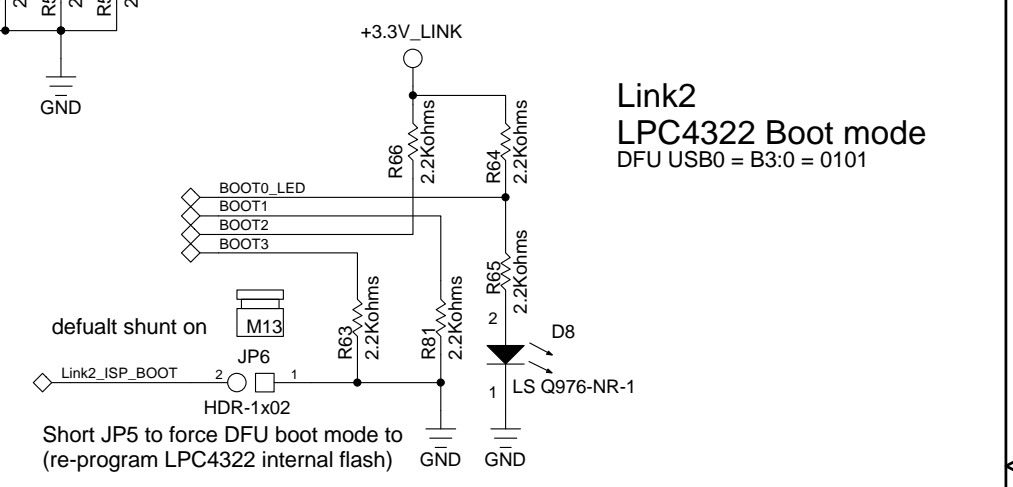
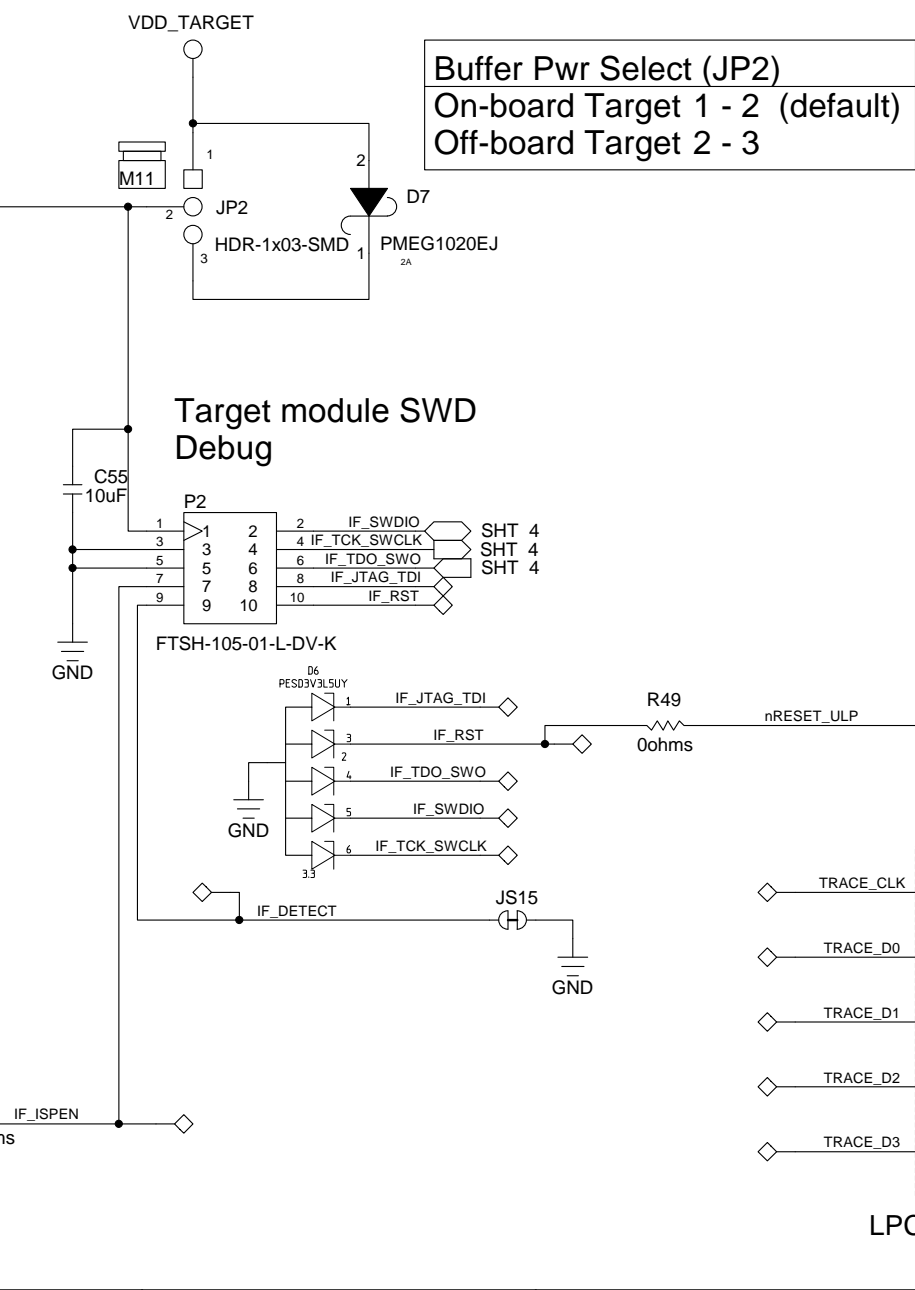
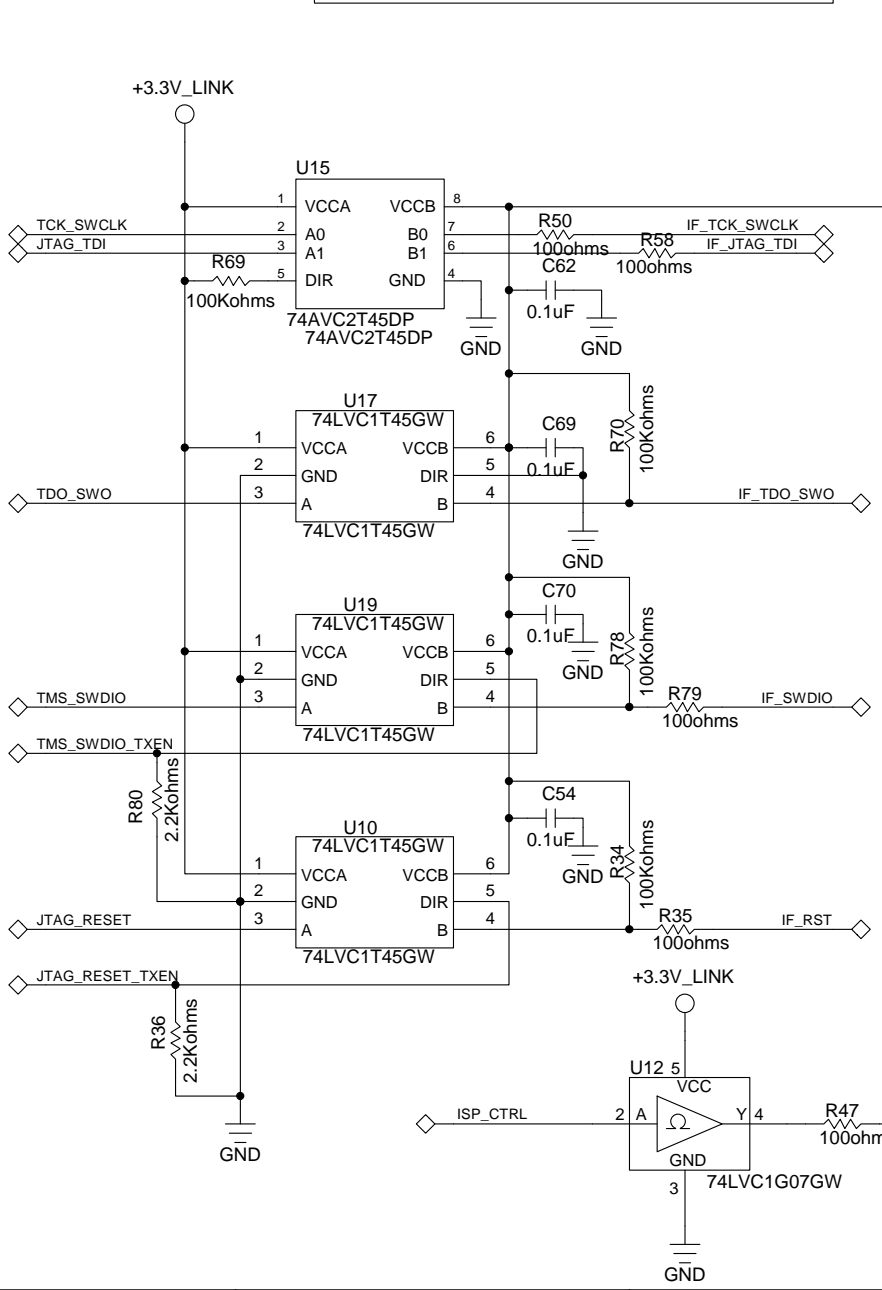
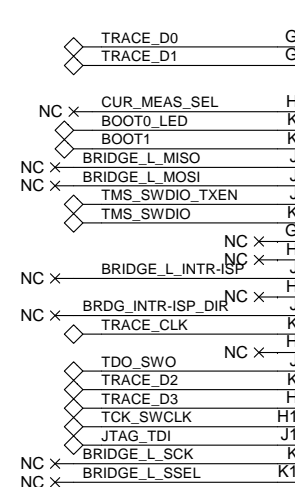
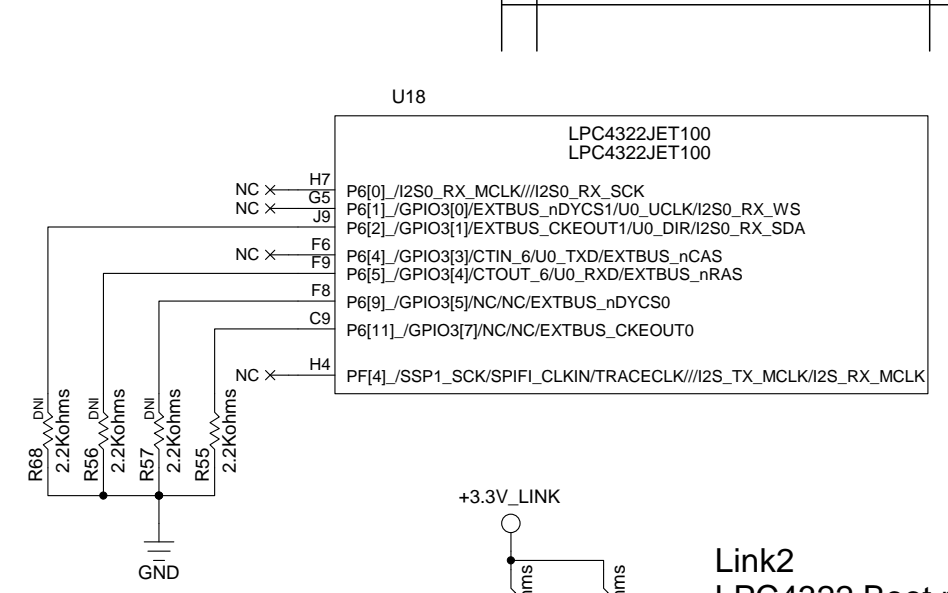
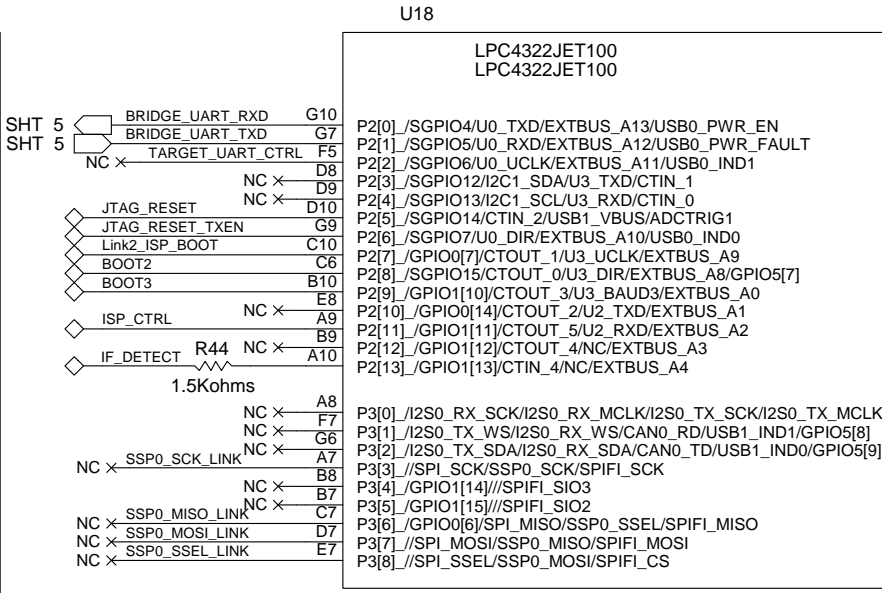
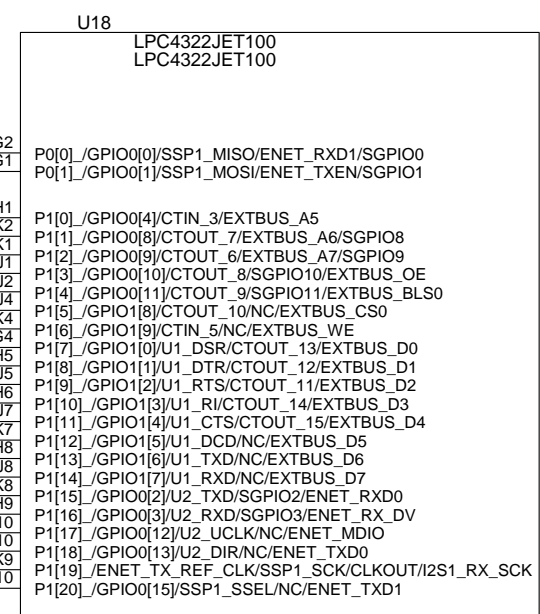
CONTRACT NO.		Audio Codec / DMIC	
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	9/20/2017		
CHECKED			
ISSUED	09/20/2017	SIZE / FSCM NO.	DWG. NO.
		D	LPC Treadstn Basebrd
		SCALE	SHEET 9 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



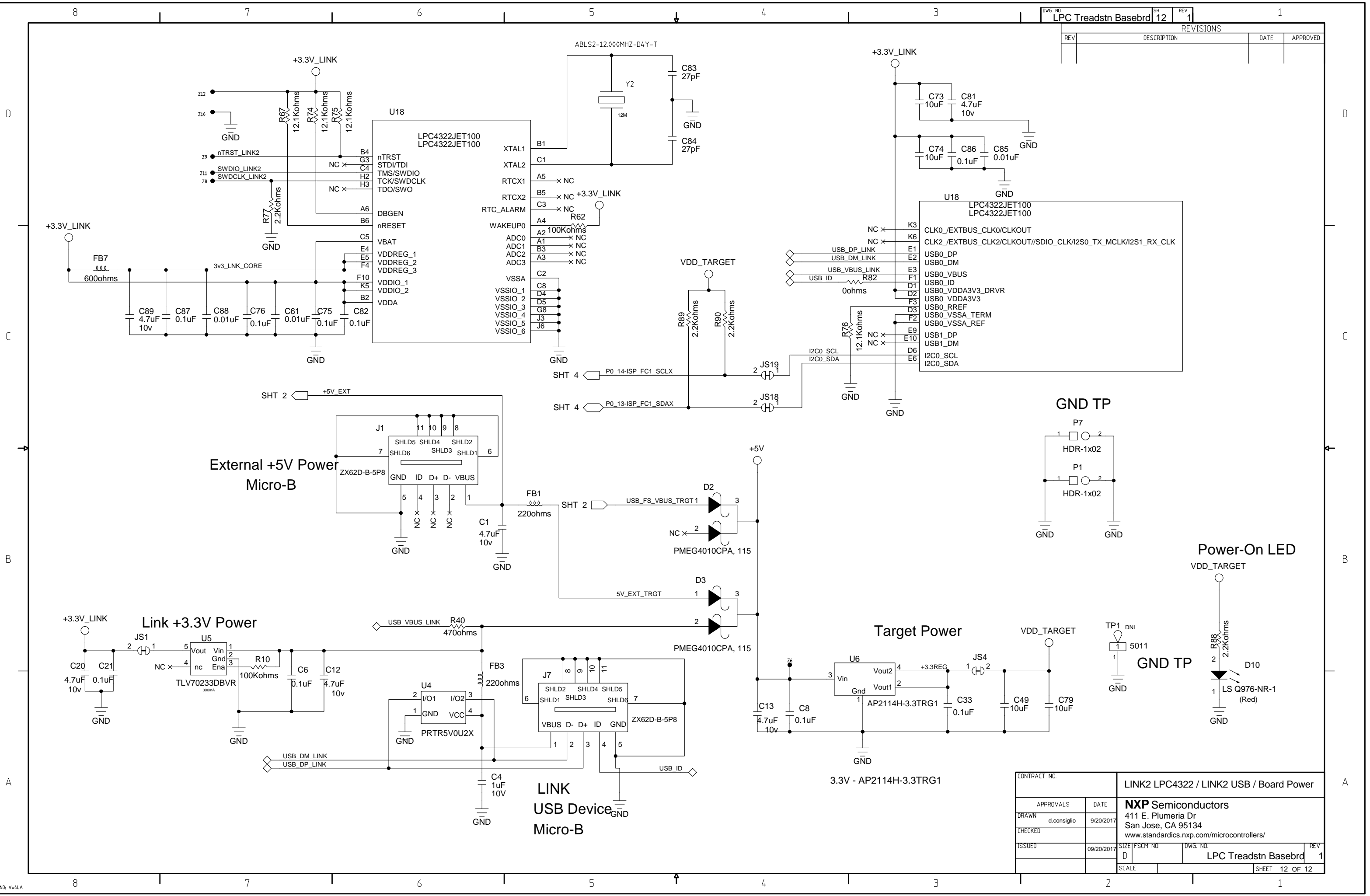
CONTRACT NO.		Shield Receptacles / Pmod / User LEDs		
APPROVALS	DATE	<b>NXP Semiconductors</b> 411 E. Plumeria Dr San Jose, CA 95134 <a href="http://www.standardics.nxp.com/microcontrollers/">www.standardics.nxp.com/microcontrollers/</a>		
DRAWN	9/20/2017			
CHECKED				
ISSUED	09/20/2017			
SIZE	D	FSCM NO.	DWG. NO.	REV
			LPC Treadstn Basebrd	1
SCALE			SHEET	10 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		LINK2 LPC4322 Peripherals / debug buffer	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	9/20/2017	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE FSCM NO.	DWG. NO.
ISSUED	09/20/2017	LPC Treadstn Basebrd	
		SCALE	SHEET 11 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		LINK2 LPC4322 / LINK2 USB / Board Power	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	9/20/2017	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	09/20/2017	www.standardics.nxp.com/microcontrollers/	
		SIZE FSCM NO.	DWG. NO.
		LPC Treadstn Basebrd	
		SCALE	SHEET 12 OF 12