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# 1 Document Revision History

<i>Revision</i>	<i>Date</i>	<i>Description</i>
PA1	2018-02-12	First version.
PA2	2018-04-17	Updated information about powering and silicon rev A0/A1.
PA3	2018-09-07	Corrected pin assignment list on pad 132.
PA4	2018-12-04	Corrected SDRAM base address.
PA5	2019-01-14	Added description for RT1062 OEM board.
PA6	2020-10-21	Corrected active polarity for PERI_PWREN.
PA7	2020-11-16	Added information about on-board pull-up resistors on GPIO_AD_B0_12 and GPIO_AD_B0_13.
A	2022-11-18	Added information about rev C1 boards, updated pinning information and Ethernet debug issue.
A1	2022-11-29	Corrected SODIMM200 pin numbers 191-198.
A2	2023-04-14	Added information about pull-up resistor on EXT_PWR_EN.
A3	2023-09-27	Corrected language in section 6.2.3.

## 2 Introduction

This document is a datasheet that specifies and describes the *iMX RT1052/62 OEM Board* mainly from a hardware point of view. Some basic software-related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

### 2.1 Hardware

The *iMX RT1052/62 OEM Board* is a Computer-on-Module (COM) based on NXP's ARM Cortex-M7 i.MX RT1052/62 microcontroller. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-M7 based design. The Cortex-M7 core runs at up to 600 MHz.

The *iMX RT1052/62 OEM Board* has a very small form factor and shields the user from a lot of complexity of designing a high-performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX RT1052/62 OEM Board* targets a wide range of applications, such as:

- Industrial Computing Designs
  - PLCs
  - Factory automation
  - Test and measurement
  - M2M
  - assembly line robotics
- Home and Building Automation
  - HVAC climate control
  - Security
  - Lighting control panels
  - IoT gateways
- Motor Control and Power Conversion
- HMI/GUI solutions
- Connected vending machines
- Access control panels
- Audio Subsystem
- 3D printers, thermal printers, unmanned autonomous vehicles
- Audio
- Smart appliances
- Home energy management systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX RT1052/62 OEM Board*.

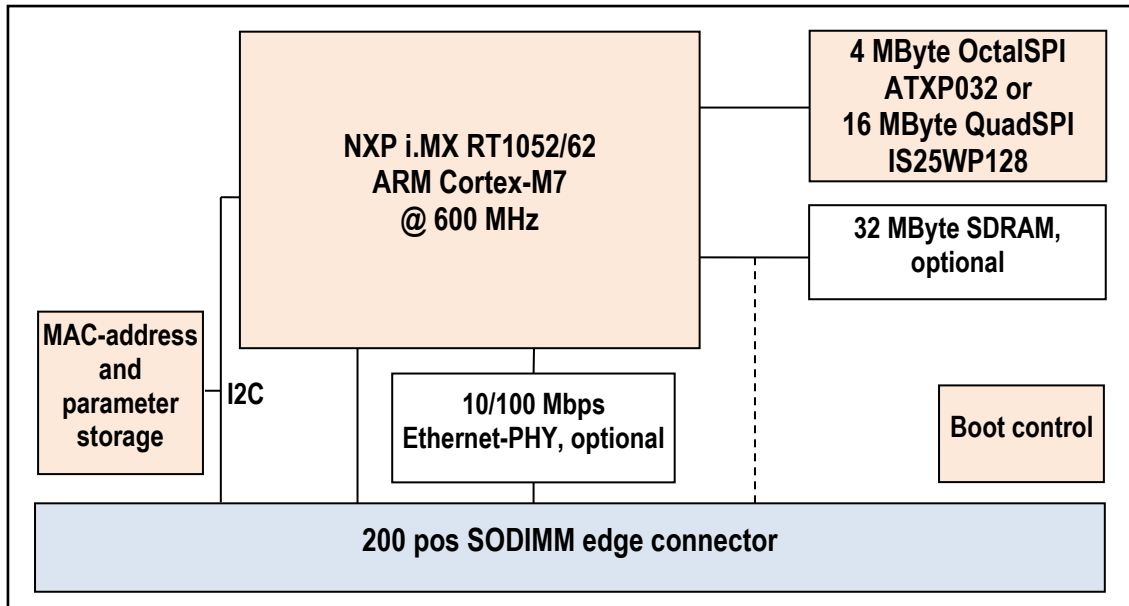


Figure 1 – iMX RT1052/62 OEM Board Block Diagram

The *iMX RT1052/62 OEM* pin assignment has been created in order to be as compatible as possible with existing OEM boards from Embedded Artists, namely the LPC1788, LPC4088 and LPC4357 OEM boards. When upgrading an existing OEM board design with the *iMX RT1052/62 OEM board* a smaller redesign of the carrier board might be needed since all alternative pin functions available are far from the same across all the OEM boards.

## 2.2 Board Versions

The *iMX RT1052/62 OEM board* comes in two main versions:

- With SDRAM - the memory bus signals (42x GPIO\_EMC) are kept local on the board and are not made available on the SO-DIMM expansion pins. This is because the high-speed signaling between the MCU and SDRAM will not tolerate stubs to a memory bus external to the board.
- Without SDRAM - the 42 GPIO\_EMC pins are available on the SO-DIMM expansion pins. This is for applications not needing the SDRAM or that need to implement a specific memory bus solution.

There are commercial and industrial temperature range boards. Note that all versions and combinations are available and/or stocked.

For high volume customers it is possible to cost optimize the boards by doing any of these options:

- remove Ethernet
- change flash memory size
- change SDRAM size

## 2.3 Software

The *iMX RT1052/62 Developer's Kit* has a Board Support Package (BSP) that supports bare metal as well as FreeRTOS based architectures. It is based on NXP's SDK framework for the i.MX RT1050/60 family with patches from Embedded Artists to support the specific flash memory mounted.

This document has a hardware focus and does not cover software development. See the document *iMX RT1052/62 Developer's Kit Program Development Guide* for more information about software development.

## 2.4 Features and Functionality

The i.MX RT1052/62 is a powerful MCU. The full specification can be found in NXP's *i.MX RT1050/60 Datasheet* and *i.MX RT1050/60 Reference Manual*. The table below lists the main features and functions of the *iMX RT1052/62 OEM board* - which represents Embedded Artists' integration of the i.MX RT1052/62 MCU. Due to pin multiplexing all functions and interfaces of the i.MX RT1052/62 may not be available at the same time. See i.MX RT1050/60 datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature	iMX RT1052/62 OEM Board
CPUs	NXP MCU <b>iMX RT1052 OEM board</b> commercial temperature range industrial temperature range	MIMXRT1052DVL6 (0 - 70° C) MIMXRT1052CVL5 (-40 - 85° C)
	NXP MCU <b>iMX RT1062 OEM board</b> commercial temperature range industrial temperature range	MIMXRT1062DVL6 (0 - 70° C) MIMXRT1062CVL5 (-40 - 85° C)
	CPU Cores	Cortex-M7 with FPU
	Maximum core frequency	600 MHz (0 - 70° C) 528 MHz (-40 - 85° C)
	L1 Instruction cache	32 KByte
	L1 Data cache	32 KByte
	I-TCM, D-TCM	Configurable, 512 KByte
	General on-chip RAM	Additional 512 KByte on i.MX RT1062 No additional RAM on i.MX RT1052
Security Functions	High Assurance Boot	✓
	Data Co-Processor (AES-128, SHA-1, SHA-256, CRC-32)	✓
	Bus Encryption Engine (AES-128, On-the-fly OctalSPI/QuadSPI decryption)	✓
	True random number generation	✓
	Secure Non-Volatile Storage	✓
	System JTAG controller	✓
Memory	SDRAM Size	32 MByte
	SDRAM RAM Speed	131 MT/s
	SDRAM RAM Memory Width	16 bit



	Flash Memory	OctalSPI 4 MByte ATXP032, or QuadSPI 16Mbyte IS25WP128
Graphical Processing	PiXel Processing Pipeline (PXP)	✓
Graphical Output	RGB, 24-bit parallel interface	✓
Graphical Input	Parallel camera, up to 24-bit parallel interface	✓
Interfaces (all functions are not available at the same time)	10/100 Mbps Ethernet-Phy (IEEE1588 compliant) One additional Ethernet interface on i.MX RT1062 - requires an external PHY	✓ with on-board PHY
	2x FlexIO (3x on i.MX RT1062)	✓
	8 ch 12-bit ADC, 4x ACMP	✓
	2x USB 2.0 OTG ports	✓
	2x SD/SDIO3.0, MMC 4.5	✓
	4x SPI, 8x UART, 4x I <sup>2</sup> C, 3x I <sup>2</sup> S/AC97	✓
	2x FlexCAN, CAN bus 2.0B (CAN-FD on i.MX RT1062)	✓
	4x FlexPWM, 4xQuadrature Encoder/Decoder	✓
Other	i.MX RT1052/62 on-chip PMIC integration with DCDC and LDO	✓
	E2PROM and MAC address	128 Byte with Ethernet MAC address
	i.MX RT1052/62 on-chip RTC	✓
	On-board watchdog functionality	✓

## 2.5 Reference Documents

The following NXP documents are important reference documents and should be consulted for functional details:

- IMXRT1050CEC, .MX RT1050 Crossover Processors for Consumer Products - Data Sheet, latest revision
- IMXRT1050IEC, .MX RT1050 Crossover Processors for Industrial Products - Data Sheet, latest revision
- IMXRT1050RM, i.MX RT1050 Processor Reference Manual, latest revision
- IMXRT1050CE, Chip Errata for the i.MX RT1050, latest revision  
**Note:** It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12094, Power consumption and measurement of i.MXRT1050, latest revision
- AN12077, Using the i.MX RT FlexRAM, latest revision

- IMXRT1060CEC, .MX RT1060 Crossover Processors for Consumer Products - Data Sheet, latest revision
- IMXRT1060IEC, .MX RT1060 Crossover Processors for Industrial Products - Data Sheet, latest revision
- IMXRT1060RM, i.MX RT1060 Processor Reference Manual, latest revision
- IMXRT1060CE, Chip Errata for the i.MX RT1060, latest revision  
**Note:** It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12253, i.MXRT1060 Product Lifetime Usage Estimates, latest revision
- AN12240, Enhanced Features in i.MX RT1060

The following documents are external industry standard reference documents and should also be consulted when applicable:

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) ([www.nxp.com](http://www.nxp.com))
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) ([www.nxp.com](http://www.nxp.com))
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture ([www.ieee.org](http://www.ieee.org))
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) ([www.sdcard.org](http://www.sdcard.org))
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia ([http://en.wikipedia.org/wiki/Serial\\_Peripheral\\_Interface\\_Bus](http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus))
- USB Specifications ([www.usb.org](http://www.usb.org))

## 3 Board Pinning

The *iMX RT1052/62 OEM* pin assignment has been created in order to be as compatible as possible with existing OEM boards from Embedded Artists, namely the LPC1788, LPC4088 and LPC4357 OEM boards.

### 3.1 Pin Numbering

The figure below illustrates the pin numbering for *iMX RT1052/62 OEM board*. It follows the JEDEC MO-224 DDR2 SO-DIMM numbering. The top side edge fingers are odd numbered 1-199. Bottom side edge fingers are even numbered 2-200.

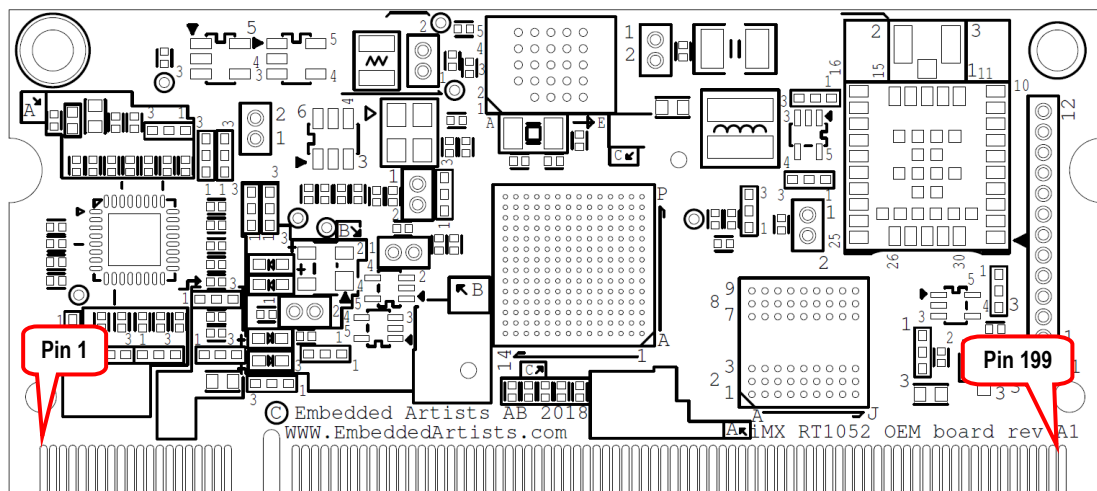


Figure 2 – iMX RT1052/62 OEM Board Pin Numbering, Top Side

### 3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

SO-DIMM pin number	Odd numbers are on the top side edge fingers and even number on the bottom side edge fingers.
OEM board function	Describe the allocated/typical usage of the pin. Some are fixed and some are programmable via different pin multiplexing options. The allocated/typical usage should be followed to get compatibility between different OEM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX RT1052/62 signal name	The name of the ball of the i.MX RT1052/62 MCU (or other component on the board) that is connected to this pin.
Alternative pin function	Indicates if the pin function is fixed or programmable via the pin multiplexing functionality of the i.MX RT1052/62 MCU.
Notes	When relevant, the preferred pin function is listed.

The table below lists all pins. Odd numbers (gray background) are on the top side and even number (white background) are on the bottom side on the board.

Note that the different mounting options and versions of the *iMX RT1052/62 OEM board* have different pins available on the SO-DIMM expansion pads. For example, the Ethernet interface pins are available when the Ethernet-Phy is not mounted, the Wi-Fi interface signals (the mounting version was only available on early prototypes) are available when the Wi-Fi module is not mounted and the memory

bus signals (GPIO\_EMC\_xxx) are available when the SDRAM is not mounted. The table also lists these differences.

SO-DIMM Pin/Pad Number	OEM Board Function	i.MX RT1052/62 Signal Name	Alternative pin functions?	Notes
1	ETH_TXP		No	Connects to on-board Ethernet-PHY.
2	ETH_RXP		No	Connects to on-board Ethernet-PHY.
3	ETH_TXN		No	Connects to on-board Ethernet-PHY.
4	ETH_RXN		No	Connects to on-board Ethernet-PHY.
5	ETH_VDD			Supply output for external Ethernet transformer.
6	ETH_GND			Connect to ground.
7	ETH_LED1		No	Connects to on-board Ethernet-PHY.
8	ETH_LED2		No	Connects to on-board Ethernet-PHY.
9	VBAT_IN	VDD_SNVIS_IN via series diode		Supply voltage from coin cell battery for keeping RTC functioning during standby.
10	-			Not connected.
11	RESET_IN		No	Reset input, active low. Pull signal low to activate a power cycle (and reset). No need to pull signal high externally.
12	RESET_OUT	POR_B buffered	No	Reset (open drain) output, active low. Driven low during reset. 1.5K pull-up resistor to VIN.
13	ENET_RST		No	The reset signal to the on-board Ethernet-Phy. This signal is controlled by GPIO_AD_B0_09, which is also the JTAG_TDI signal. It can be useful to be able to access this signal during JTAG debug. See section 9.3 for details.  <b>Note: this pin is only connected on rev C1 boards (EAC00428). On other board revisions, this pin is not connected.</b>
14	JTAG_DBGEN	GPIO_AD_B0_08	Yes	Pull low to enable JTAG interface. Board has 10K pulldown on this signal.
15	JTAG_TCK	GPIO_AD_B0_07	Yes	
16	-			Not connected.
17	JTAG_TRST	GPIO_AD_B0_11	Yes	
18	JTAG_TMS	GPIO_AD_B0_06	Yes	
19	JTAG_TDI	GPIO_AD_B0_09	Yes	<b>Note that this signal is connected to the Ethernet-Phy reset. This can cause issues during JTAG debug. See section 9.3 for details.</b>
20	JTAG_TDO	GPIO_AD_B0_10	Yes	<b>Note that this signal is connected to the Ethernet-Phy interrupt signal. This can cause issues during JTAG debug. See section 9.3 for details.</b>
21	VDD_ADC	VDDA_ADC_3P3	No	Supply output for ADC reference supply. Do not source more than 10 mA from this supply.
22	-			Not connected.
23	GND			Connect to ground.
24	GND			Connect to ground.
25		GPIO_AD_B0_04	Yes	This is boot control signal BOOT_MODE0. The signal shall not be driven from an external source. The signal can be used as an output.  <b>Note that this signal has an on-board 33K ohm pull-down resistor. The boot control logic can drive this signal high or low via a 4.7K ohm resistor.</b>
26	ENET_IRQ			The interrupt signal from the on-board Ethernet-Phy. It is connected to GPIO_AD_B0_10, which is the JTAG_TDO signal. It can be useful to be able to access this signal during JTAG debug. See

section 9.3 for details.

Note: this pin is only connected on rev C1 boards (EAC00428). On other board revisions, this pin is not connected.

27	LCD_DCLK	GPIO_B0_00	Yes	
28	LCD_VSYNC	GPIO_B0_03	Yes	
29	LCD_DEN	GPIO_B0_01	Yes	
30	LCD_HSYNC	GPIO_B0_02	Yes	
31	LCD_D12	GPIO_B1_00	Yes	
32	LCD_D13	GPIO_B1_01	Yes	
33	LCD_D14	GPIO_B1_02	Yes	
34	LCD_D15	GPIO_B1_03	Yes	
35	ISP_ENABLE		No	Pull low to enable USB OTG bootloader at boot. Signal has 50Kohm pullup on board. See section 6.5 for details.
36	USBA_VBUS	USB_OTG1_VBUS		VBUS input for USB channel#1/A
37	VIN			Main 3.3V input.
38	GND			Connect to ground.
39	VIN			Main 3.3V input.
40	GND			Connect to ground.
41	USBB_DP	OTG2_DP	No	
42	USBA_DP	OTG1_DP	No	
43	USBB_DN	OTG2_DN	No	
44	USBA_DN	OTG1_DN	No	
45	LCD_D11	GPIO_B0_15	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
46	LCD_D0	GPIO_B0_04	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
47	CAN_RD	GPIO_AD_B0_15	Yes	
48	CAN_TD	GPIO_AD_B0_14	Yes	
49	UART_TXD	GPIO_AD_B0_12	Yes	There is a 10K ohm pull-up resistor to 3.3V on this signal.
50	UART_RXD	GPIO_AD_B0_13	Yes	There is a 10K ohm pull-up resistor to 3.3V on this signal.
51	-			Not connected.
52	-			Not connected.
53	-			Not connected.
54	-			Not connected.
55	-			Not connected.
56	-			Not connected.
57		GPIO_AD_B1_10	Yes	
58		GPIO_AD_B1_11	Yes	
59		GPIO_AD_B0_02	Yes	
60		GPIO_AD_B0_03	Yes	
61		GPIO_AD_B0_01	Yes	
62		GPIO_AD_B0_00	Yes	
63	-			Not connected.
64	-			Not connected.
65	-			Not connected.

66	-			Not connected.
67	-			Not connected.
68	-			Not connected.
69	-			Not connected.
70		GPIO_AD_B1_08	Yes	
71	-			Not connected.
72	-			Not connected.
73		GPIO_B1_12	Yes	
74	I2C_SDA	GPIO_AD_B1_01	No	2K2ohm pullup to VIN. Must be I2C1_SDA.
75	I2C_SCL	GPIO_AD_B1_00	No	2K2ohm pullup to VIN. Must be I2C1_SCL.
76	GND			Connect to ground.
77	GND			Connect to ground.
78	SD_CLK	GPIO_SD_B0_01	Yes	
79	SD_CMD	GPIO_SD_B0_00	Yes	
80	SD_PWREN	GPIO_AD_B0_05	Yes	<p>This is boot control signal BOOT_MODE1. The signal shall not be driven from an external source. The signal can be used as an output.</p> <p>Note that this signal has an on-board 33K ohm pull-down resistor. The boot control logic can drive this signal high or low via a 4.7K ohm resistor.</p>
81	SD_D0	GPIO_SD_B0_02	Yes	
82	SD_D1	GPIO_SD_B0_03	Yes	
83	SD_D2	GPIO_SD_B0_04	Yes	
84	SD_D3	GPIO_SD_B0_05	Yes	
85	SD_VCC	NVCC_SD	No	Supply voltage for SD interface (1.85V or 3.2V). Should only supply the SD interface.
86		GPIO_B1_15	Yes	
87		GPIO_B1_14	Yes	
88	LCD_D5	GPIO_B0_09	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
89	LCD_D6	GPIO_B0_10	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
90	LCD_D7	GPIO_B0_11	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
91	LCD_D8	GPIO_B0_12	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
92	LCD_D9	GPIO_B0_13	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
93	LCD_D10	GPIO_B0_14	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
94	LCD_D1	GPIO_B0_05	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
95	LCD_D2	GPIO_B0_06	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
96	LCD_D3	GPIO_B0_07	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
97	LCD_D4	GPIO_B0_08	Yes	Note that this signal has an on-board 10K ohm pull-down resistor.
98	USBB_VBUS	USB_OTG2_VBUS	No	VBUS input for USB channel#2/B
99	-			Not connected.
100	WDOG_B		No	Watchdog input, active low. Pull signal low to activate a power cycle (and reset).
101	GND			Connect to ground.
102	GND			Connect to ground.
103		GPIO_AD_B1_14	Yes	

104		GPIO_AD_B1_13	Yes	
105		GPIO_AD_B1_15	Yes	
106	-			Not connected.
107		GPIO_SD_B1_04	Yes	Note that the logic level for this pin is 1.8V (not 3.3V as it is for all other GPIO pins).
108		GPIO_AD_B1_12	Yes	
109		POR_B	No	Direct POR_B input to i.MX RT1052/62
110		ONOFF	No	Direct connection to i.MX RT1052/62 signal ONOFF.
111		OTG1_CHD	No	Direct connection to i.MX RT1052/62 signal OTG1_CHD.
112		WAKEUP	No	Direct connection to i.MX RT1052/62 signal WAKEUP.
113	-			Not connected.
114	-			Not connected.
115		GPIO_AD_B1_09	Yes	
116		PMIC_ON_REQ	No	Direct connection to i.MX RT1052/62 signal PMIC_ON_REQ.
117	EXT_PWR_EN		No	Open-drain output to control external power supply for VIN. The signal is active high and <b>requires an external pull-up resistor. See iMX OEM Carrier Board schematic for a reference implementation.</b>
118	PERI_PWREN	PMIC_STBY_REQ	No	Direct connection to i.MX RT1052/62 signal PMIC_STBY_REQ.  Output to control external peripherals connected to i.MX RT1052/62 I/O pins. Signal is active low - when external peripherals may drive i.MX RT1052/62 I/O signals. Signal is high when external driving of signals is not allowed (to prevent powering back-feed). The signal can also be used to save power by power-down of external circuits. See iMX OEM Carrier Board schematic for a reference implementation (via a PMOSFET).
119		GPIO_B1_13	Yes	
120		(GPIO_AD_B1_02)	(Yes)	Signal is only available on boards without Wi-Fi module.
121		(GPIO_AD_B1_03)	(Yes)	Signal is only available on boards without Wi-Fi module.
122		(GPIO_AD_B1_04)	(Yes)	Signal is only available on boards without Wi-Fi module.
123		(GPIO_AD_B1_05)	(Yes)	Signal is only available on boards without Wi-Fi module.
124		(GPIO_AD_B1_06)	(Yes)	Signal is only available on boards without Wi-Fi module.
125		(GPIO_AD_B1_07)	(Yes)	Signal is only available on boards without Wi-Fi module.
126		CCM_CLK1_N	No	Direct connection to i.MX RT1052/62 signal CCM_CLK1_N.
127	BOOT_CTRL		No	This is a boot control input. See section 6.5 for details.  Note that this pin was introduced on boards with revision B1/B2 and forward. On earlier board revisions, this pin was unconnected.
128		CCM_CLK1_P	No	Direct connection to i.MX RT1052/62 signal CCM_CLK1_P.
129	GND			Connect to ground.
130	GND			Connect to ground.
131		(GPIO_EMC_39)	(Yes)	Signal is only available on boards without SDRAM.
132		(GPIO_EMC_38)	(Yes)	Signal is only available on boards without SDRAM.
133		(GPIO_EMC_26)	(Yes)	Signal is only available on boards without SDRAM.
134		(GPIO_EMC_8)	(Yes)	Signal is only available on boards without SDRAM.
135		(GPIO_EMC_27)	(Yes)	Signal is only available on boards without SDRAM.
136		(GPIO_EMC_24)	(Yes)	Signal is only available on boards without SDRAM.
137		(GPIO_EMC_20)	(Yes)	Signal is only available on boards without SDRAM.

138	(GPIO_EMC_25)	(Yes)	Signal is only available on boards without SDRAM.
139	(GPIO_EMC_19)	(Yes)	Signal is only available on boards without SDRAM.
140	(GPIO_EMC_22)	(Yes)	Signal is only available on boards without SDRAM.
141	(GPIO_EMC_23)	(Yes)	Signal is only available on boards without SDRAM.
142	(GPIO_EMC_21)	(Yes)	Signal is only available on boards without SDRAM.
143	(GPIO_EMC_18)	(Yes)	Signal is only available on boards without SDRAM.
144	(GPIO_EMC_28)	(Yes)	Signal is only available on boards without SDRAM.
145	(GPIO_EMC_17)	(Yes)	Signal is only available on boards without SDRAM.
146	(GPIO_EMC_29)	(Yes)	Signal is only available on boards without SDRAM.
147	(GPIO_EMC_16)	(Yes)	Signal is only available on boards without SDRAM.
148	(GPIO_EMC_41)	(Yes)	Signal is only available on boards without Ethernet-Phy.
149	(GPIO_EMC_15)	(Yes)	Signal is only available on boards without SDRAM.
150	(GPIO_EMC_40)	(Yes)	Signal is only available on boards without Ethernet-Phy.
151	(GPIO_EMC_14)	(Yes)	Signal is only available on boards without SDRAM.
152	(GPIO_B1_04)	(Yes)	Signal is only available on boards without Ethernet-Phy.
153	(GPIO_EMC_13)	(Yes)	Signal is only available on boards without SDRAM.
154	(GPIO_B1_05)	(Yes)	Signal is only available on boards without Ethernet-Phy.
155	(GPIO_EMC_12)	(Yes)	Signal is only available on boards without SDRAM.
156	(GPIO_B1_06)	(Yes)	Signal is only available on boards without Ethernet-Phy.
157	(GPIO_EMC_11)	(Yes)	Signal is only available on boards without SDRAM.
158	(GPIO_B1_07)	(Yes)	Signal is only available on boards without Ethernet-Phy.
159	(GPIO_EMC_10)	(Yes)	Signal is only available on boards without SDRAM.
160	(GPIO_B1_08)	(Yes)	Signal is only available on boards without Ethernet-Phy.
161	(GPIO_EMC_9)	(Yes)	Signal is only available on boards without SDRAM.
162	(GPIO_B1_09)	(Yes)	Signal is only available on boards without Ethernet-Phy.
163	(GPIO_B1_11)	(Yes)	Signal is only available on boards without Ethernet-Phy.
164	(GPIO_B1_10)	(Yes)	Signal is only available on boards without Ethernet-Phy.
165	VIN_ALWAYS ON		Always-on 3.3V supply.
166	GND		Connect to ground.
167	(GPIO_EMC_37)	(Yes)	Signal is only available on boards without SDRAM.
168	GND		Connect to ground.
169	(GPIO_EMC_36)	(Yes)	Signal is only available on boards without SDRAM.
170	GND		Connected to ground on rev C1 boards. Not connected on other revisions.
171	(GPIO_EMC_35)	(Yes)	Signal is only available on boards without SDRAM.
172	GND		Connected to ground on rev C1 boards. Not connected on other revisions.
173	(GPIO_EMC_34)	(Yes)	Signal is only available on boards without SDRAM.
174	GND		Connected to ground on rev C1 boards. Not connected on other revisions.
175	(GPIO_EMC_33)	(Yes)	Signal is only available on boards without SDRAM.
176	GND		Connected to ground on rev C1 boards. Not connected on other revisions.
177	(GPIO_EMC_32)	(Yes)	Signal is only available on boards without SDRAM.



178	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
179		(GPIO_EMC_31)	(Yes)	Signal is only available on boards without SDRAM.
180	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
181		(GPIO_EMC_30)	(Yes)	Signal is only available on boards without SDRAM.
182	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
183		(GPIO_EMC_7)	(Yes)	Signal is only available on boards without SDRAM.
184	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
185		(GPIO_EMC_6)	(Yes)	Signal is only available on boards without SDRAM.
186	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
187		(GPIO_EMC_5)	(Yes)	Signal is only available on boards without SDRAM.
188	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
189		(GPIO_EMC_4)	(Yes)	Signal is only available on boards without SDRAM.
190	GND			Connected to ground on rev C1 boards. Not connected on other revisions.
191		(GPIO_SD_B1_00)	(Yes)	Note: Connected to signal GPIO_SD_B1_00 on rev C1 boards.
		(GPIO_EMC_3)	(Yes)	Note: Connected to signal GPIO_EMC_3 on rev A2 and B2 boards (boards without SDRAM).
192	-			Not connected.  The pin was originally allocated for the on-board Wi-Fi/BT module, but this mounting option is now obsolete.
193		(GPIO_SD_B1_01)	(Yes)	Note: Connected to signal GPIO_SD_B1_01 on rev C1 boards.
		(GPIO_EMC_2)	(Yes)	Note: Connected to signal GPIO_EMC_2 on rev A2 and B2 boards (boards without SDRAM).
194	-			Not connected.  The pin was originally allocated for the on-board Wi-Fi/BT module, but this mounting option is now obsolete.
195		(GPIO_SD_B1_02)	(Yes)	Note: Connected to signal GPIO_SD_B1_02 on rev C1 boards.
		(GPIO_EMC_1)	(Yes)	Note: Connected to signal GPIO_EMC_1 on rev A2 and B2 boards (boards without SDRAM).
196	-			Not connected.  The pin was originally allocated for the on-board Wi-Fi/BT module, but this mounting option is now obsolete.
197		(GPIO_SD_B1_03)	(Yes)	Note: Connected to signal GPIO_SD_B1_03 on rev C1 boards.
		(GPIO_EMC_0)	(Yes)	Note: Connected to signal GPIO_EMC_0 on rev A2 and B2 boards (boards without SDRAM).
198	-			Not connected.  The pin was originally allocated for the on-board Wi-Fi/BT module, but this mounting option is now obsolete.
199	-			Not connected.  The pin was originally allocated for on-board Wi-Fi/BT module powering, but this mounting option is now obsolete.
200	GND			Connect to ground.

## 4 Pin Mapping

### 4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX RT1052/62 MCU. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many alternative functions. This leaves great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like clock outputs and USB. Pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between OEM boards, keep the OEM specified pin allocation, but in general there are no restrictions to select alternative pin multiplexing schemes on the *i.MX RT1052/62 OEM Board*.

Functional multiplexing is normally controlled via the SDK BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_XXX` where `XXX` is the name of the i.MX RT1052/62 pin. For more information about the register settings, see the *i.MX RT1050/60 Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_XXX_SELECT_INPUT` where `XXX` is the name of the input function. Again, for more information about the register settings, see the *i.MX RT1050/60 Processor Reference Manual* from NXP.

#### 4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the OEM function allocation. The reset state is typically GPIO, ALT5 function.

### 4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the SDK BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_XXX` where `XXX` is the name of the i.MX RT1052/62 pin. For more information about the register settings, see the *i.MX RT1050/60 Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, with a keeper functionality (a few has pull-down resistor), after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

## 5 Memory Areas

This chapter presents the different memories that are available.

### 5.1 FlexRAM - Internal 512 KByte RAM

The large 512 KByte internal RAM of the i.MX RT1052/62 is controlled by the FlexRAM block. It is highly configurable and flexible. The 512 KByte array is divided into sixteen 32 KByte blocks. Each of these blocks can be configured as one of three functions:

- OCRM (On-Chip RAM memory)
- DTCM (Data Tightly-Coupled Memory)
- ITCM (Instruction Tightly-Coupled Memory)

Configuration is controlled either by an otp fuse value, which is the default, or by software via register IOMUXC\_GPR\_GPR16 and IOMUXC\_GPR\_GPR17. The FlexRAM banks can be configured at runtime.

The default value, no otp fuses set, is the following memory allocation: 256 KByte to OCRM, 128 KByte each to DTCM and ITCM.

The memory address region for RAM blocks configured as OCRM is: 0x2020 0000

The memory address region for RAM blocks configured as DTCM is: 0x2000 0000

The memory address region for RAM blocks configured as ITCM is: 0x0000 0000

There is an application note: *Using the i.MX RT FlexRAM* (AN12077) that describes the FlexRAM block in more detail. This is recommended reading.

### 5.2 On-chip RAM - Additional 512 KByte RAM on i.MX RT1062

There is an additional 512 kByte OCRM block available on the i.MX RT1062.

### 5.3 External FLASH

On board versions up to rev B1 and B2, there is an external 4 Mbyte OctalSPI flash has memory address region: 0x6000 0000 - 0x603F FFFF

On board versions from C1, there is an external 16 Mbyte QuadSPI flash has memory address region: 0x6000 0000 - 0x60FF FFFF

### 5.4 External 32 MByte SDRAM

The external SDRAM has memory region: 0x8000 0000 - 0x81FF FFFF (32 MByte)

### 5.5 E2PROM with MAC Address

There is a 128 Byte E2PROM with MAC address (EUI-48) connected to I2C channel#1. The 8-bit I2C address is 0xA6/0xA7 (read/write), which equals to a 7-bit I2C address of 0x53.

The memory is 24AA025E48T from Microchip.

## 6 Integration - Carrier Board Design

This chapter describes the essential steps of integrating the iMX RT1052/62 OEM board into a custom design. This involves designing a custom carrier board. Best practice tips are also given.

The *iMX Carrier board* design is a reference implementation of a carrier board.

### 6.1 Pin Multiplexing

One of the first thing to do when creating a design around the *iMX RT1052/62 OEM board* is to allocate peripheral blocks and associated pins to the external interfaces. The two document *i.MX RT1050/60 Crossover Processor Datasheet* (document id: IMXRT1050CEC / IMXRT1060CEC and IMXRT1050IEC / IMXRT1060IEC) and *i.MX RT1050/60 Processor Reference Manual* (document id: IMXRT1050RM / IMXRT1060RM) should always be consulted for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

There is an accompanying Excel document that lists all alternative functions for each available I/O pin (with pin multiplexing options). This is an excellent help for funding a suitable pin allocation.

### 6.2 Powering

The iMX RT1052/62 OEM board needs a number of power supplies, as illustrated in the picture below.

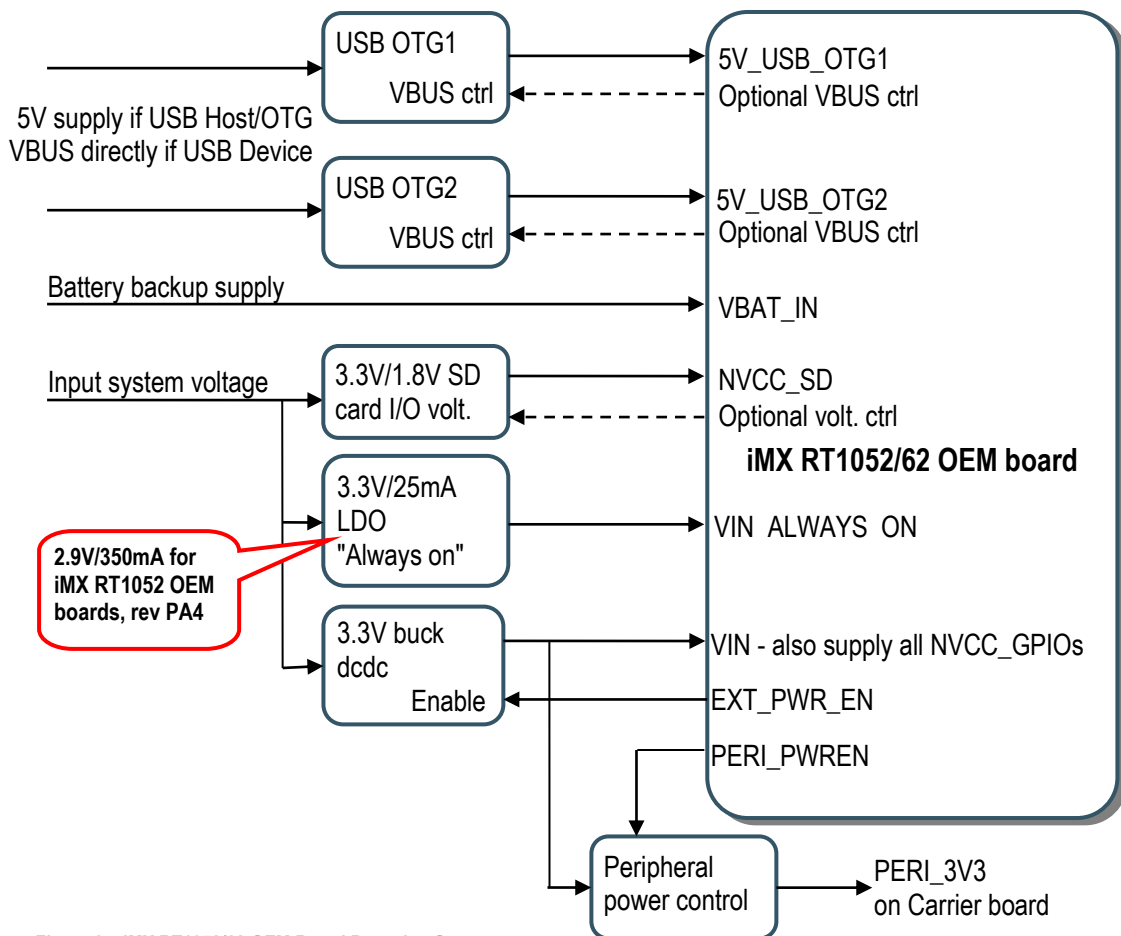


Figure 3 – iMX RT1052/62 OEM Board Powering Structure

There are two main supplies:

- VIN, which is a 3.3V supply that is controlled by the signal EXT\_PWR\_EN (active high – **but an open-drain output so it requires an external pull-up resistor**). This power supply is typically a buck dc/dc converted since it also powers 3.3V peripherals on the carrier board.
- VIN\_ALWAYS\_ON, which is also a 3.3V supply but the difference from VIN is that this supply shall always be present. This supply can with advantage be an LDO in order to lower standby current in the lowest power consumption modes.

This supply will keep the on-board RTC running and the ONOFF function active.

VIN\_ALWAYS\_ON connected (via a Schottky diode) directly to the VDD\_SNVS\_IN supply input of the i.MX RT1052/62 MCU. If VIN\_ALWAYS\_ON is not powered, the RTC will be powered via VBAT\_IN.

- Note that on iMX RT1052/62 OEM boards, rev A (and later) the supply shall be 3.3V and be able to supply 25mA.
- Note that on iMX RT1052 OEM boards, rev PA4 this supply shall be 2.9V and be able to supply 350mA. This is due to a powering errata on the i.MX RT1052 silicon revision A0.

In addition to above, VBAT\_IN can optionally be supplied to keep the real-time clock (RTC) and ONOFF functionality active even if VIN and VIN\_ALWAYS\_ON are removed. VBAT\_IN connected (via a Schottky diode) directly to the VDD\_SNVS\_IN supply input of the i.MX RT1052/62 MCU. If VBAT\_IN is not powered, the RTC will be powered via VIN\_ALWAYS\_ON.

VBAT\_IN and VIN\_ALWAYS\_ON power the VDD\_SNVS\_IN supply input of the i.MX RT1052/62 MCU in parallel. Only one of these supplies is needed. Depending on the carrier board design and general powering architecture of the overall system, either VBAT\_IN and VIN\_ALWAYS\_ON are used.

The power supply shall be designed for the maximum current consumption of the *OEM Board* and should be able to deliver this at the maximum temperature for the system. The current consumption very much depends on how the MCU and memories on the OEM board are used. Current consumption is for example much higher when program executes from external SDRAM than from internal SRAM. Usage of Ethernet, USB and FLASH also affect current consumption. For simplicity, the power supply can be designed for the maximum current consumption listed in this datasheet. For designs requiring a more optimized design, it is recommended to measure the current consumption with the final application running. Then design the power supply with some reasonable margin.

#### 6.2.1 Optional Adjustable SD Interface Powering

The NVCC\_SD supply input can either be connected directly to VIN (3.3V) or an optional 3.3V/1.8V adjustable voltage regulator. The latter is only needed if a more advanced memory card interface (UHS-I) is needed.

#### 6.2.2 USB Interface Powering

The two USB interface supply inputs must also be powered if they are active. For a USB Host or OTG interface, connect a +5V supply from a distribution switch (to VBUS of the USB interface). For a USB Device interface, just connect to VBUS of the USB interface.

Each of the USB\_OTGx\_3P3 supply inputs can consume up to 25mA max for an active interface.

#### 6.2.3 Peripheral Supply Control

**No I/O pins should be externally driven while the I/O power supply (VIN, which is connected internally to the NVCC\_GPIO supply) is OFF.** That can cause internal latch-up and malfunctions due to reverse current flows.

First of all, always power all external peripherals via 3V3\_MAIN (see the iMX OEM Carrier Board schematic for reference – U1 is a 3.3V power supply controlled by signal EXT\_PWR\_EN).

By powering all circuits on the carrier board via 3V3\_MAIN, there is no risk to drive any of the GPIO pins on the iMX RT1052/62 when not allowed to.

Optionally also power gate the 3V3\_MAIN supply (to the peripheral circuit on the carrier board) with the PERI\_PWREN signal. See the *iMX OEM Carrier board* design for a reference implementation of this. The PERI\_PWREN output is active low. The signal can be used to shut down (i.e., power save) certain peripherals on the carrier board.

### 6.3 Reset

It is possible to control the POR\_B signal directly (via SODIMM pin 109), but it is not needed. There is an internal reset generator that reacts on the VIN supply input.

There is no need from the *iMX RT1052/62 OEM board* perspective to have an external reset signal. If there is an additional external reset source, the RESET\_IN signal can be driven with an open-drain driver.

### 6.4 External Memory Bus

On *iMX RT1052/62 OEM boards* without SDRAM it is possible to create an external memory bus with the GPIO\_EMC\_xxx signals. Such a bus must be very carefully designed. The total length must be minimized. All signals must be length matched. Exact number for this depends on the frequency the bus will run on but at highest speed (>100 MHz all signals must be within 50 mil). No (or very short) stubs are allowed. All signals should be routed with 50 ohm impedance to ground (preferred, but VIN will also work). Switching between reference plane (ground or VIN) is not recommended.

Note that on *iMX RT1052/62 OEM boards* with SDRAM it is not possible to expand the memory bus. The GPIO\_EMC\_xxx signals are not available on the SO-DIMM connector pads. The reason for this is that external stubs on the high-frequency content signals will create too reflections, which will severely negatively affect the signal integrity of the memory bus to operate correctly.

### 6.5 Booting Options

The i.MX RT1052/62 MCU can boot from multiple sources and there are two different ways to control this; either via boot configuration pins or internal OTP fuses. There is also a USB OTG boot mode that is commonly referred to as "Serial Download" or "Recovery" mode. This latter mode is used during development and in production to download the first binary image (often a first stage bootloader). It is typically not used by the end-product during normal operation.

The *iMX RT1052/62 OEM board* is designed to boot from the on-board OctalSPI/QuadSPI flash memory by default. Since the *iMX RT1052/62 OEM board* is delivered without any internal otp fuses set, the boot mode is set to "internal boot" meaning that the boot mode configuration is controlled by the boot configuration pins. These pins (GPIO\_B0\_04 to GPIO\_B0\_15, LCDIF\_D0 to LCDIF\_D11) must not be driven externally when the board comes out of reset. Design the system so that GPIO\_B0\_04 to GPIO\_B0\_15 are outputs and not driven by any external circuits. Their default level is low (pulled low by on-board 10Kohm resistors) and this works well if the pins are for example LCD data outputs.

The *iMX RT1052/62 OEM board* has two input signals to control the boot mode, BOOT\_CTRL and ISP\_ENABLE, see table below:

Boot source	BOOT_CTRL	ISP_ENABLE
<b>Boot from on-board OctalSPI/QuadSPI flash</b> The board boots according to the default settings of signals GPIO_B0_04 to GPIO_B0_15, LCDIF_D0 to LCDIF_D11, which have	Floating	Floating

<p>been setup to boot from the on-board OctalSPI/QuadSPI flash.</p> <p>Note that these signals (GPIO_B0_04 to GPIO_B0_15) may not be driven externally just after reset.</p> <p><b>If any of the signals are driven externally (or a different boot source than OctalSPI/QuadSPI is needed) then this boot mode cannot be used. Instead, program the on-chip OTP fuses for the wanted boot source.</b></p>		
<p><b>Boot according to OTP fuses (eFuses)</b></p> <ul style="list-style-type: none"> <li>Any boot mode supported by the i.MX RT1052/62 MCU and the hardware connected to it can be selected. See <i>IMXRT1050RM, i.MX RT1050 Processor Reference Manual</i>, latest revision or <i>IMXRT1060RM, i.MX RT1060 Processor Reference Manual</i>, latest revision for details about boot sources and OTP fuse settings.</li> </ul> <ol style="list-style-type: none"> <li>Note that OTP fuse BT_FUSE_SEL must be set to 1 to have OTP fuse settings controlling boot source. If not set to 1, the USB OTG boot mode (aka "Serial download") is activated.</li> <li>Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery.</li> <li><i>iMX RT1052/62 OEM boards</i> are delivered without programmed on-chip OTP fuses. Users have full control over these.</li> </ol>	Low (grounded)	Floating
<p><b>USB OTG</b></p> <p>This is known as "Serial Download" or "Recovery" mode.</p> <p>This mode is used during development and in production to download the first image (typically a first stage bootloader). It is typically not used by the end-product during normal operation.</p> <p>This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.</p>	Do not care	Low (grounded)

The two control signals BOOT\_CTRL and ISP\_ENABLE are not directly connected to i.MX RT1052/62 pins. Instead, they control the two boot mode signals of the i.MX RT1052/62 MCU; GPIO\_AD\_B0\_04 and GPIO\_AD\_B0\_05. Design the system so that GPIO\_AD\_B0\_04 and GPIO\_AD\_B0\_05 are outputs and not driven by any external circuits.

i.MX RT1052/62 Signal	Boot mode pin	Signal level for "Internal boot" mode, which is default	Signal level when Boot according to OTP fuses (eFuses)	Signal level for "USB OTG boot", which is active then signal ISP_ENABLE is pulled low
GPIO_AD_B0_04	BOOT_MODE0	Low	Low	High
GPIO_AD_B0_05	BOOT_MODE1	High	Low	Low

## 6.6 Best Practice

This section presents a number of best practice recommendations for custom carrier board designs.



### 6.6.1 Follow the iMX OEM Carrier Board schematic

The iMX OEM Carrier Board schematic is a reference implementation of the different interfaces. Follow this design to get the different interfaces implemented correctly. This is especially true around the powering of the iMX RT1052/62 OEM board.

### 6.6.2 Add JTAG Debug Interface

To support proper debugging with a JTAG probe a Cortex debug interface should always be implemented on the carrier board design. If there is no space for it in the final product, at least add the debug interface on a break-off part of the board (that is only used during initial development).

The pads for the debug interface components/connector can be left on the final board but not just populated on volume production boards (to save cost).

Also, always add ESD protection to the debug interface. It is interface that can get used a lot is often forgotten to protect.

It is also recommended to add support for more advanced debugging with the SWO trace signal. Note that the i.MX RT1052/62 MCU does not connect the SWO trace output signal on signal JTAG\_TDO, which would be the normal (since JTAG\_TDO connect to the Cortex debug connector pin 6 where SWO is defined to be connected). Instead, pin GPIO\_B0\_13 carries the SWO output as pin multiplexing alternative 2. The solution is to add an optional selector jumper so either JTAG\_TDO or signal GPIO\_B0\_13 can be routed to pin 6 of the Cortex debug connector.

### 6.6.3 Watchdog

Add the watchdog setup that has been created in NXP's BSP software by connecting pin WDOG\_B (SO-DIMM pin 100) with GPIO\_B1\_13 (SO-DIMM pin 119) via a zero ohm resistor.

A negative edge on the signal (high-to-low) will trigger a power cycle in the system.

If the watchdog functionality is not used, just do not populate the zero ohm resistor that connects the two pins.

### 6.6.4 Application Download During Production

There are two ways to download the application code into the OctalSPI/QuadSPI flash memory during production; either via the JTAG debug interface or via USB OTG boot mode.

It is recommended to always add the JTAG debug interface, simply to have the possibility to properly debug the application.

It is also recommended to add support for the USB OTG boot mode by implementing USB channel#1 as a USB device/otg interface. Also add the possibility to pull signal ISP\_ENABLE low, which is what will enable the USB OTG bootloader to be activated after a power cycle.

If the USB OTG boot mode is not used in production of in the final application, just do not populate these components on the boards being produced in volume.

### 6.6.5 Access to UART Channel

Another useful recommendation to simplify program development is to add a UART "console" channel, where debug information can be routed to.

### 6.6.6 Add Series Resistors for Current Measurement

It is good practice to add series resistors on the power supply rails to the different loads in the system. Sometimes it is helpful to understand where the current consumption is in the system, especially when debugging low-power applications.

The series resistors can be populated with zero ohm resistors in the normal case, and be replaced with low ohm resistors when measuring currents. Note the maximum current rating of smaller resistors. Sometimes 0603 or 0805 sized zero ohm resistors must be selected because of max current rating.



Add small access pads around the series resistors to simplify voltage measurement over the resistors. If there is space, add a 2-position 100 pin pitch pin header. Some debug probes (for example MCU-Link-Pro or ULINKplus) have current measurement connectors with 100 mil pitch.

#### 6.6.7 I2C Isolation

It is recommended to add series resistors on the I2C channel (SCL/SDA) to each I2C node. If there is a problem with one particular node during development, it can easily be disconnected and no longer disturbs the I2C communication.

### 6.7 SO-DIMM Connector and OEM board Mounting

Section 7.6 specify the mechanical measurement. It also specifies the SO-DIMM connector standard to use (DDR2 SO-DIMM according to the JEDEC MO-224 standard). A right-angled connector is recommended. Make sure to verify that the selected SO-DIMM connector is the "1.8V keying".

There are two mounting holes on the *iMX RT1052/62 OEM board*. Add associated mounting holes on the carrier board if vibration can occur in the system.

### 6.8 Verify Operating Conditions

Self-heating in an application can sometimes be significant (depending on ventilation and cooling). Always measure the operating temperature on the i.MX RT1052/62 MCU under worst case situations (lowest temperature, no execution activity versus highest temperature, maximum execution). Verify that the case temperature is within margins of the *iMX RT1052/62 OEM board* used.

The i.MX RT1052/62 MCU self-heats about 23-25 degrees Celsius. Operating above 75 degrees Celsius will require heat management since the processor will shut down (thermal shutdown) when the junction temperature reaches 105 degrees Celsius.

Also make sure the relative humidity (RH) limits are met. The non-condensing requirement is important to meet. This can be a problem if the temperature in the system varies rapidly.

### 6.9 ESD/EMI Protection

In general, it is very important to protect a design from the effects of ESD and EMI. External signals entering the carrier board, and eventually the *iMX RT1052/62 OEM board*, must be properly protected from both ESD and EMI. It is very application dependent what type of protection is needed. Different standards can be consulted for details about needed protection.

### 6.10 CE Directive

The goal of electromagnetic compatibility (EMC) is correct operation of a system (immunity of EMI) and the avoidance of generating unwanted effects to other systems (emission of EMI).

The *iMX RT1052/62 OEM board* is classified as a component and is hence not CE marked separately. It can perform different functions in different integrations, and it does not have a direct function. It is therefore not in the scope of the CE Directive. An end product, where an *iMX RT1052/62 OEM board* is integrated into, is however very likely to need CE marking.

The *iMX RT1052/62 OEM board* has been designed according to best practice for reducing electromagnetic emission with multilayer PCB, appropriate decoupling, component placement and trace routing. Measurements must however be performed on the final products and the result very much depends on the environment into which it is integrated to. Shielding around the product might be needed for compliance.

### 6.11 Powering Errata on i.MX RT1052 Silicon Revision A0

Note that there is a serious errata related to powering on i.MX RT1052 silicon revision A0. Failure to observe these can result in irreversible damage to the i.MX RT1052 MCU.

**Embedded Artists' iMX RT1052 OEM board, revision PA4 are built with silicon revision A0 of the i.MX RT1052 MCU. These boards are affected by the power related errata.**

Embedded Artists' iMX RT10522 OEM board, revision A (and later) are built with silicon revision A1 of the i.MX RT1052 MCU. These boards are shipped from April 2018. These boards will not be affected by the power related errata. Note however that there can be other erratas on the MCU that are not addressed in this section.

On iMX RT1052 OEM board, revision PA4 the secondary/always-on supply voltage **MUST** be 2.9V instead of 3.3V and **MUST** have higher current rating (350 mA) than normally needed (typically 100 mA). It **MUST** also start up before the main 3.3V power supply. Also note that the debug probe I/O voltage **MUST** follow the i.MX RT1052 I/O voltage. The debug adapter must not drive any output higher than the Vcc/Vref voltage (and if that voltage is zero, then the debug adapter must not drive any output signal).

Failure to follow any of these four MUSTs will cause the i.MX RT1052 MCU to not startup properly and possibly be irreversibly damaged.

**By following the powering solution of the iMX Carrier board design the MUSTs listed above are meet.**

Make sure the debug probe does not have a fixed output voltage, but rather follow Vcc/Vref. If using LPC-Link2 as debug interface, make sure there is NO jumper inserted in JP2. For other debug probes, check the documentation carefully.

**It is our recommendation to only design your custom carrier board around iMX RT1052 OEM boards, based on silicon A1, that is board revision A (or later).**

**Also note that there is no similar powering errata on the iMX RT1062 OEM board.**

## 7 Technical Specification

### 7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
<b>VIN</b>	Main input supply voltage	-0.3	3.6	V
<b>VIN_ALWAYS</b>	Input supply voltage, always on (silicon rev A1) <sup>[1]</sup>	-0.3	3.6	V
<b>VBAT</b>	RTC supply voltage	-0.3	3.6	V
<b>VIO</b>	Vin/Vout (I/O VDD + 0.3): 3.3V IO	-0.5	3.6	V
<b>USB_OTGx_VBUS</b>	USB VBUS signals	-0.3	5.5	V

<sup>[1]</sup> VIN\_ALWAYS Input supply voltage, always on (silicon rev A0): -0.3V to 3.0V

### 7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
<b>VIN</b>	Main input supply voltage	3.2	3.3	3.4	V
	Ripple with frequency content < 10 MHz			50	mV
	Ripple with frequency content ≥ 10 MHz			10	mV
<b>VIN_ALWAYS</b> <sup>[2]</sup>	Input supply voltage, always on (silicon rev A1) <sup>[3]</sup>	3.2	3.3	3.4	V
	Ripple with frequency content < 10 MHz			50	mV
	Ripple with frequency content ≥ 10 MHz			10	mV
<b>VBAT</b> <sup>[2]</sup>	RTC supply voltage (VDD_SNVS_IN)	2.8	3.3	3.6	V
<b>USB_OTGx_VBUS</b>	USB VBUS signals	4.4	5	5.5	V

<sup>[2]</sup> Either VIN\_ALWAYS or VBAT must be present (and within valid range) for correct operation of the board (including, but not limited, the ONOFF functionality and the RTC).

<sup>[3]</sup> Input supply voltage, always on (i.MX RT1052 silicon rev A0, not applicable to RT1062): 2.9V ±0.1V

### 7.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN, VIN\_ALWAYS and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-50 ms.

**VIN\_ALWAYS shall be high/valid before VIN is ramped up.**

### 7.4 Electrical Characteristics

For DC electrical characteristics, see i.MX RT1052 MCU Datasheet. Depending on internal VDD operating point, OVDD is identical to VIN.

#### 7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN. Maximum output voltage when active is 0.4V.

### 7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 20  $\mu$ S minimum. The internal reset pulse will be 140-280 mS long, before the i.MX RT1052/62 boot process starts.

## 7.5 Power Consumption

There are several factors that determine power consumption of the *iMX RT1052/62 OEM board*, like input voltage, operating temperature, SDRAM activity, operating frequency of the core, Ethernet activity and software executed.

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate. Supply voltage is 3.3V and all currents (VIN, VIN\_ALWAYS ON and VBAT) are summed to one number.

Symbol	Description (VIN = VIN_ALWAYS ON = 3.3V, Toperating = 25°C)	Typical	Unit
I <sub>VIN_MAX</sub>	Maximum CPU load, 600 MHz core frequency	200	mA
I <sub>VIN_SYSDLE</sub>	System idle state	10	mA
I <sub>VIN_LPIDLE</sub>	Low power idle state	2.5	mA
I <sub>VIN_SUSPEND</sub>	Suspend state	260	$\mu$ A
I <sub>VBAT_RTC</sub>	Current consumption to keep internal RTC running	20	$\mu$ A

## 7.6 Mechanical Dimensions

The board uses the DDR2 SO-DIMM mechanical form factor.

Dimension	Value ( $\pm 0.1$ mm)	Unit
Module width	67.6	mm
Module height	30	mm
Module top side height	2.2 Can be up to 3.0	mm
Module bottom side height	1.3 Can be up to 1.7	mm
PCB thickness	1.0	mm
Mounting hole diameter	2.5	mm
Module weight (without Wi-Fi module)	6 $\pm$ 1 gram	gram

The **DDR2 SO-DIMM** standard is also called to be 200-pos SO-DIMM connector that is 1.8V keyed. The JEDEC standard defining the DDR2 SO-DIMM boards is called **JEDEC MO-224** and it is connectors supporting this standard that shall be used.

Note that there are also 2.5V keyed SO-DIMM boards and these are called DDR1 SO-DIMM boards. These connectors cannot be used.

A typical DDR2 SO-DIMM socket specifications looks like below (with minor variations between different models):

- Durability: 25 Cycles

- Voltage Rating: 25VAC
- Current Rating: 0.5A
- Contact Resistance: 50mΩ max.
- Dielectric Withstanding Voltage: 250V AC/1 min.
- Insulation Resistance: 50MΩ
- Operating Temperature: -40°C to +85°C

There are several different connectors from manufacturers like TE Connectivity AMP Connectors, Foxconn and FCI.

The picture below illustrates the mechanical details of the 67.6 x 30 mm module, including the antenna connector position (for boards with Wi-Fi module mounted).

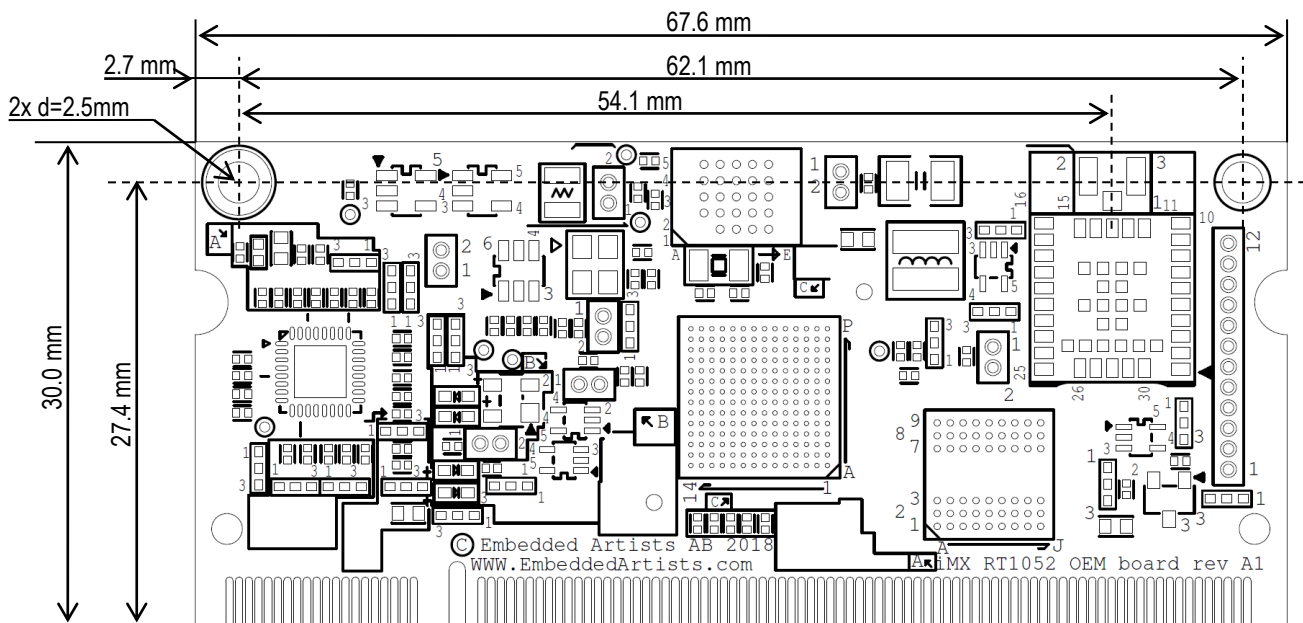


Figure 4 – iMX RT1052/62 OEM Board Mechanical Outline

### 7.6.1 SO-DIMM Socket

The board has 200 edge fingers that mates with an DDR2 SO-DIMM connection, which is a low profile 200 pos, 0.6mm pitch right angle connector on the carrier board. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.7 mm.

The 1565917-4 connector from TE Connectivity AMP Connectors is used by Embedded Artists. This connector gives a board-to-board stacking height of 2.9 mm. This space allows some components to also be placed right under the OEM board.

Always check available component height before placing components on the carrier board under the OEM board, see picture below.

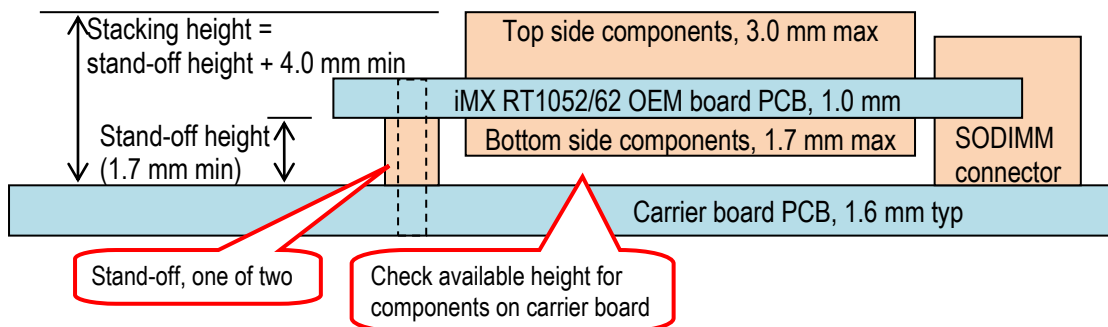


Figure 5 – OEM Board Mounting in DDR SO-DIMM Connector, Stacking Height

### 7.6.2 Board Assembly Hardware

The carrier board can have two M2 threaded stand-offs for securing the *iMX RT1052/62 OEM board* to the SO-DIMM connector and carrier board. Check needed stand-off height and screw length, depending on selected SO-DIMM connector.

## 7.7 Environmental Specification

### 7.7.1 Operating Temperature

Ambient temperature ( $T_A$ )

Parameter	Min	Max	Unit
Operating temperature range:	commercial temperature range		0 70 <sup>[1]</sup> °C
	industrial temperature range		-40 85 <sup>[1]</sup> °C
Storage temperature range	-40	85	°C
Junction temperature i.MX RT1052/62 MCU, operating:	comm. temp. range		0 95 °C
	ind. temp. range.		-40 105 °C

<sup>[1]</sup> Depends on cooling solution. If natural convection is used, junction temperature must be below limit.

### 7.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , non-condensing (comm. temp. range)	10	80	%
Operating: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , non-condensing (ind. temp. range)			
Non-operating/Storage: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , non-condensing	5	90	%

## 7.8 Thermal Design Considerations

Heat dissipation from the i.MX RT1052/62 MCU depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat is typically less than 0.5 Watt. Note that an active Ethernet-Phy can have considerable heat dissipation. This must be considered also.

Whether external cooling is needed, or not, depends on dissipated heat, ambient temperature range and air flow. In most cases it is possible to operate the *iMX RT1052/62 OEM Board* without external cooling. If natural convection is used care must be taken so that junction temperature is below the limit. There is a 20-degree Celsius margin from 85 degrees (highest temperature for industrial operating temperature range) to 105 degrees (highest silicon junction temperature). Note that the i.MX RT1052/62 MCU self-heats about 23-25 degrees Celsius under normal operating conditions.

**Operating above 75 degrees Celsius will require heat management, i.e., transfer heat from the processor.**

The i.MX RT1052/62 MCU has an integrated temperature sensor for monitoring the junction (i.e., die) temperature. It will shut down/reset the processor when the junction temperature reaches 105 degrees Celsius.

### 7.8.1 Thermal Parameters

The i.MX RT1052/62 MCU thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ( $R_{\theta JA}$ ), natural convection	43.9	°C/W
Thermal Resistance, CPU Junction to package top ( $\psi_{JT}$ )	0.6	°C/W

## 7.9 Product Compliance

Visit Embedded Artists' website at [http://www.embeddedartists.com/product\\_compliance](http://www.embeddedartists.com/product_compliance) for up-to-date information about product compliances such as CE, RoHS2/RoHS3, Conflict Minerals, REACH, etc.

## 8 Functional Verification and RMA

The *iMX RT1052/62 Developer's Kits* come with a pre-loaded demo/test application. It is described in the document *iMX RT1052/62 Developer's Kits User's Guide*. This application can be used to troubleshoot a board that does not seem to operate properly. Note that these tests must be performed on the *iMX OEM Carrier board* that comes with the *iMX RT1052/62 Developer's Kit*.

It is strongly advised to perform these tests before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document

([http://www.embeddedartists.com/sites/default/files/docs/General\\_Terms\\_and\\_Conditions.pdf](http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf)).



## 9 Things to Note

This chapter presents several issues and considerations that users must note.

### 9.1 Shared Pins and Multiplexing

The i.MX RT1052/62 MCU has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX RT1052/62 OEM* on-board design. Check if the needed interfaces are available to allocation before starting a design. There is a separate Excel sheet for this, showing all the pin multiplexing options available for each signal on the SODIMM200 expansion connector.

### 9.2 Handling SO-DIMM Boards

See picture below for instructions about how to mount/remove the *OEM Board* in the SO-DIMM connector of the *iMX OEM Carrier Board*.

To install the *OEM Board*, align it to the socket (1). Push the board gently, and with even force between the board edges, fully into the socket (2). Then push the board down in a rotating move (3) until it snaps into place (4). The *OEM Board* shall lie flat and parallel to the base board.

To remove the *OEM Board*, spread the two arms of the SO-DIMM socket apart slightly. The board will pop up (5). Gently raise the board in a rotating move (6) and then extract the board from the socket (7). Apply even force between board edges when removing so that the board is removed parallel to the locking arms.

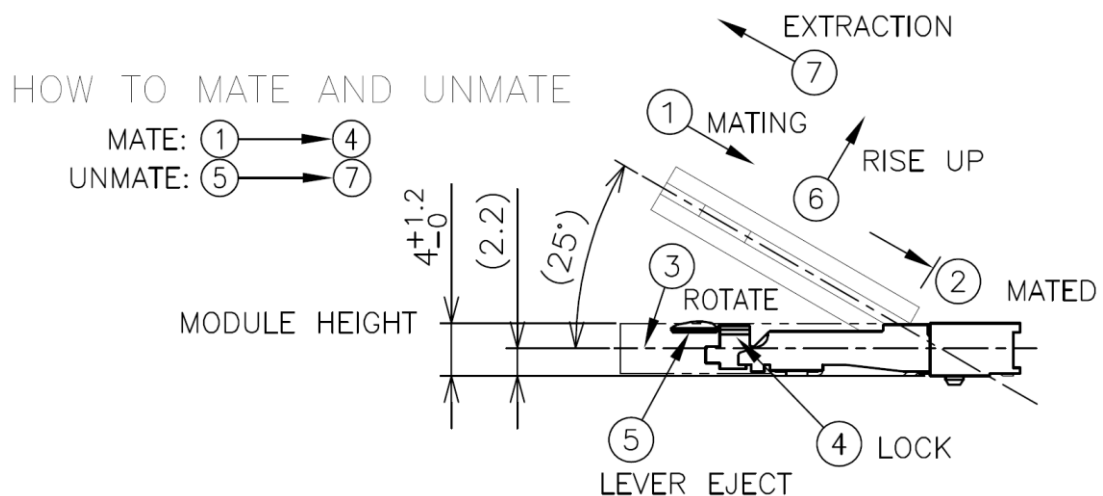


Figure 6 – Instructions how to Mount/Remove an OEM Board

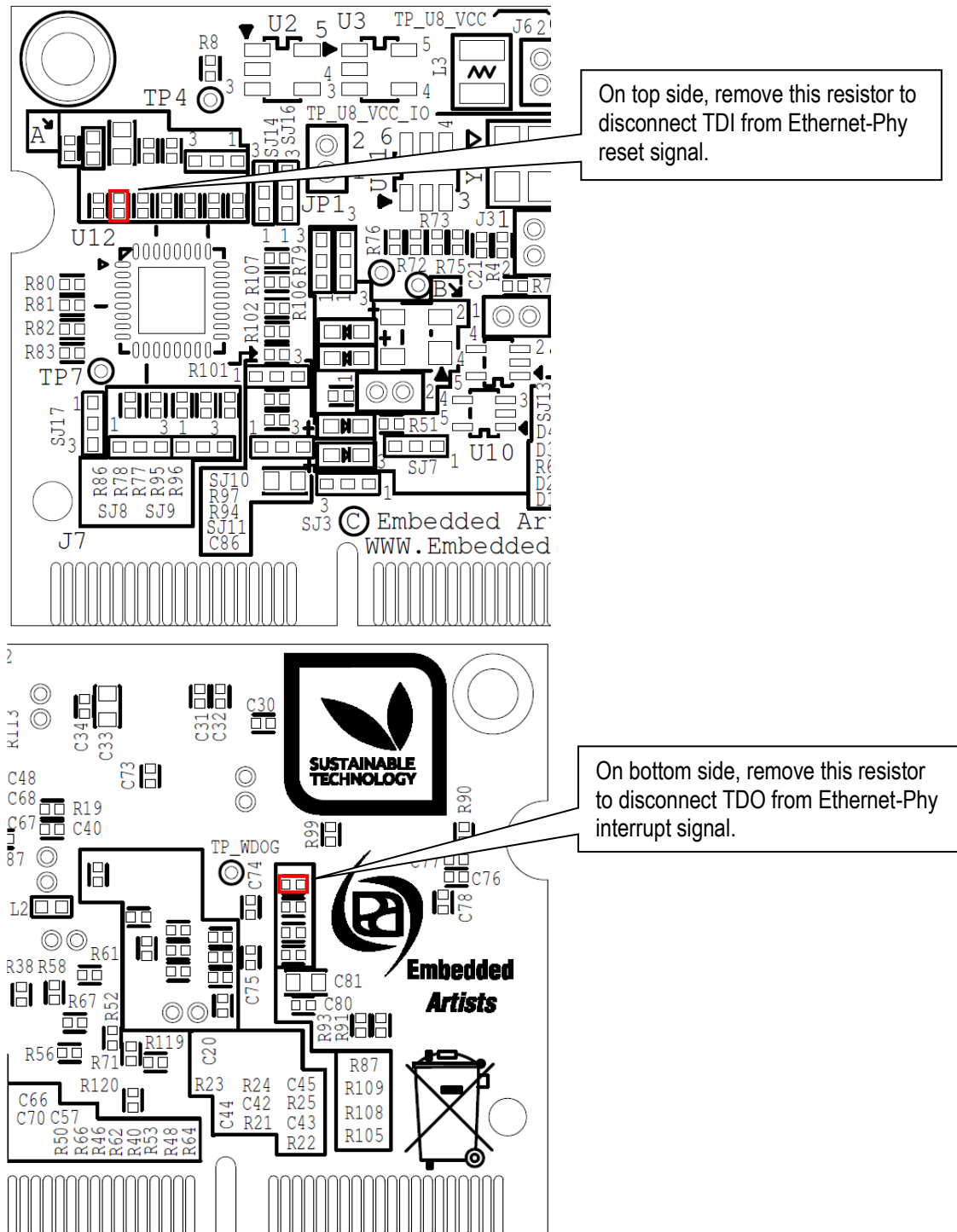
Do not forget to follow standard ESD precaution routines when mounting/removing the *OEM Board*. Most signals exposed on the 200 edge contact fingers on the SO-DIMM board are unprotected. Maintain the same electrical potential of the *OEM Board* (to be mounted) and the base board. Do not touch the *OEM Board* edge connectors. Handle the *OEM Board* only by the three other edges. Also, do not touch the components on the board.

### 9.3 Ethernet-Phy not working while JTAG Debugging

The Ethernet-Phy reset and interrupt signals are connected to the JTAG TDI/TDO signals. When debugging via JTAG, the Ethernet interface will not be operating properly because of this.

It is possible to disconnect the JTAG TDI/TDO signals from the Ethernet-Phy by removing two resistors. In most cases it is possible to operate the Ethernet interface without the reset and interrupt signals, at least during debug sessions. The Ethernet-Phy signals can be accessed on SODIMM200 pin 13 and 26 on rev C1 boards, if access to these signals is needed.

Below is a rework instruction to disconnect signals JTAG\_TDI and JTAG\_TDO from the Ethernet-Phy.



## 9.4 Program Content when OEM Boards are Delivered

The *iMX RT1052/62 OEM* board is delivered with a pre-programmed application that is just a forever loop of NOP operations. No pin initialization is done so the application mimics what happens if the program flash would be empty or if USB Boot loader/ISP mode is enabled.

Note that in general **it is a bad idea to assume the *iMX RT1052/62 OEM* board is always unprogrammed/empty when you first mount in on a carrier board**. The board can have been accidentally programmed with another application during the program development work.

It is strongly recommended to implement a procedure to always make sure a known application is programmed to an *iMX RT1052/62 OEM* board when mounted on a carrier board. Before powering a board that has just been mounted on a carrier board, place the processor in USB Boot loader/ISP mode (by pulling pin ISP\_Enable low). Design the carrier board so that a processor in USB Boot loader mode/ISP will not be damaged or do anything harmful to the carrier board. Program the correct application directly after powering the carrier board (with the new *iMX RT1052/62 OEM* board).

**Note** that when the *iMX RT1052/62 OEM* board is sold as part of an *iMX RT1051/62 Developer's Kit*, a demo application is programmed to the board. This is one of the reasons to never assume an *iMX RT1052/62 OEM* board does not have an application programmed.

## 9.5 OTP Fuse Programming

The *iMX RT1052/62 MCU* has on-chip OTP fuses that can be programmed, see NXP documents *IMXRT1050RM / IMXRT1060RM*, *iMX RT1050/60 Processor Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

*iMX RT1052/62 OEM Boards* are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses should be programmed and, in that case, which ones.

**Note that Embedded Artists does not replace *iMX RT1052/62 OEM Boards* because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.**

## 9.6 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX RT1052/62 OEM Board* targets a wide range of applications, such as:

- Industrial Computing Designs
  - PLCs
  - Factory automation
  - Test and measurement
  - M2M
  - assembly line robotics
- Home and Building Automation
- HVAC climate control
- Security
- Lighting control panels
- IoT gateways
- Motor Control and Power Conversion
- HMI/GUI solutions
- Connected vending machines

- Access control panels
- Audio Subsystem
- 3D printers, thermal printers, unmanned autonomous vehicles
- Audio
- Smart appliances
- Home energy management systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For harsher use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exist, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX RT1052/62 OEM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. To ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX RT1052/62 OEM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

**The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX RT1052/62 OEM Board*.**

### 9.7 ESD Precaution when Handling iMX RT1052/62 OEM Board

Please note that the *iMX RT1052/62 OEM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.



***Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards.*** That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the boards to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

**Note that Embedded Artists does not replace boards that have been damaged by ESD.**

### 9.8 EMC / ESD

The *iMX RT1052/62 OEM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless, depending on the target system, additional anti-interference measurement may still be necessary to adhere to the limits for the overall system.

The *iMX RT1052/62 OEM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only make sense on the complete solution.

No specific ESD protection has been implemented on the *iMX RT1052/62 OEM Board*. ESD protection on board level is the same as what is specified in the i.MX RT1052/62 MCU datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

## 10 Custom Design

This document specifies the standard *iMX RT1052/62 OEM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different memory sizes on SDRAM and serial Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove SDRAM and/or Ethernet interface.
- Different pinning on SODIMM edge pins.
- Different board form factor.
- Different input supply voltage range, for example 5V input.
- Single Board Computer solutions, where the core design of the *iMX RT1052/62 OEM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

## 11 Different Board Versions

The different board versions, flash, silicon versions and MCU top side marking have overlapping and sometimes confusing versions numbers. Therefore, this chapter contains information about different board versions, flash memory and i.MX RT1052/62 silicon versions.

iMX RT1052 OEM Board version and part number	i.MX RT1052 Silicon Version	Flash	i.MX RT1052 Top Marking
iMX RT1052 OEM Board, rev PA4 (EAC00295)	A0	OctalSPI ATXP032	PIMXRT1052DVL6A (comm.) PIMXRT1052CVL5A (ind.)
iMX RT1052 OEM Board, rev A1 and A2 Rev A1 is a board with SDRAM (EAC00306) Rev A2 is a board without SDRAM (EAC00305)	A1	OctalSPI ATXP032	MIMXRT1052DVL6B (comm.) MIMXRT1052CVL5B (ind.)

iMX RT1062 OEM Board version and part number	i.MX RT1062 Silicon Version	Flash	i.MX RT1062 Top Marking
iMX RT1062 OEM Board, rev A1 and A2 Rev A1 is a board with SDRAM (EAC00308) Rev A2 is a board without SDRAM (EAC00309)	A0	OctalSPI ATXP032	PIMXRT1062DVL6A (comm.) PIMXRT1062CVL5A (ind.)
iMX RT1062 OEM Board, rev B1 and B2 Rev B1 is a board with SDRAM (EAC00308) Rev B2 is a board without SDRAM (EAC00309)	A0 A1	OctalSPI ATXP032 OctalSPI ATXP032	MIMXRT1062CVL5A (ind.) MIMXRT1062CVL5B (ind.)
iMX RT1062 OEM Board, rev C1 Rev C1 is a board with SDRAM (EAC00428) No board version without SDRAM has been created	A1	QuadSPI IS25WP128	MIMXRT1062CVL5B (ind.)

### 11.1 Rev C1 Board Differences

There are several small differences between older board revisions and the new rev C1 revision:

- Flash: The older (now obsolete) 4 Mbyte OctalSPI ATXP032 has been replaced with 16 Mbyte QuadSPI IS25WP128.
- Ethernet-Phy reset signal is available on SODIMM200 pin 13.
- Ethernet-Phy interrupt signal is available on SODIMM200 pin 26.
- Signal GPIO\_SD\_B1\_00 connected to SODIMM200 pin 191.
- Signal GPIO\_SD\_B1\_01 connected to SODIMM200 pin 193.
- Signal GPIO\_SD\_B1\_02 connected to SODIMM200 pin 195.
- Signal GPIO\_SD\_B1\_03 connected to SODIMM200 pin 197.
- SODIMM-200 pins 168, 170, 172, 174, 176, 178, 180, 182, 184, 186, 188, 190 are grounded.

## 12 Disclaimers

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Embedded Artists does not accept any liability and no warranty is given for any unexpected software behavior due to deficient components.

Customer is required to take note of manufacturer's specification of used components, for example MCU, SDRAM and FLASH. Such specifications, if applicable, contains additional information that must be taken note of for the safe and reliable operation. These documents are stored on Embedded Artists' product support page.

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